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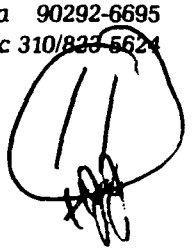

Sponsored by Advance Projects Agency
ARPA/CSTO

ARPA/CSTO RAPID VLSI IMPLEMENTATION

Final Technical Report

Date of Report: July 1993

Title of Contract: Rapid VLSI Implementation
Project: VLSI Prototyping Project
ARPA Order No: 6132

Issued by: AFCMD/KCC
Under Contract Number: F29601-87-C-0069
Period of Performance: 09/28/87 - 09/30/91

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August 18, 1993

LtCol John Toole, Deputy Director
ARPA/CSTO
3701 N. Fairfax DR.
Arlington, VA 22203-1714

SUBJECT: Final Technical Report for Rapid VLSI Implementation
CONTRACT NO.: F29601-87-C-0069

Dear LtCol Toole:

Please find enclosed two (2) copies of the Final Technical Report and Form DD-250 for the period covering 09/28/87 - 09/30/91 in accordance with the reporting requirements as stated in the subject contract. Please note that this report is Approved for Public Release and Distribution is Unlimited.

Sincerely yours,

Beverly Ann Hartmeyer
Contract Manager

BAH:mj

Enclosures:

cc: Defense Technical Information Center (12 Copies)
ARPA/ISTO (2 Copies)
USC Dept. of Contracts and Grants
File: VLSI

FINAL REPORT FOR EFFORT OF OCTOBER 1,1987 THROUGH SEPTEMBER 30, 1991

ORGANIZATION: INFORMATION SCIENCES INSTITUTE, UNIVERSITY OF SOUTHERN CALIFORNIA

PRINCIPAL INVESTIGATOR: César Piña, CPINA@MOSIS.EDU, Ph 3108221511

TITLE OF EFFORT: MOSIS MICROELECTRONICS BROKERAGE SERVICE

I. TASK OBJECTIVE:

To provide rapid access to cost effective, state of the art US Microelectronics Industry fabrication technology for DoD customers and the educational community. This access was provided through the establishment of a prototyping service for use by the DARPA and NSF research communities which offered access to a variety of technologies unobtainable from a single fabrication source. The Defense Advanced Research Projects Agency (DARPA) had the goal of providing state-of-the-art VLSI fabrication services and electronic systems assembly technology to DoD customers and the educational community to ensure that DoD has access to low-cost, advanced electronic assemblies, and to ensure that the country's newly emerging engineers will be able to support military needs in the area of electronics. The first task was to provide VLSI fabrication to DoD and DARPA supported contractors who have need of custom chips and assemblies. The second task was to provide this same technology to NSF-sponsored activities, under DARPA guidance.

II. TECHNICAL PROBLEM

1.0 COSTS

One of the main problems facing a researcher who needs to access state of the art IC fabrication technology, is the high cost of individual (dedicated) fabrication runs. To a first order approximation, the cost of a project to the user is equal to the cost of the fabrication run divided by the number of users in the run. Unfortunately, for dimensions smaller than 2um, use of stepper based technology becomes essential, if any sort of a reasonable yield is to be obtained. In stepper based technology, the majority of the wafer fabricators employ reticles having dimensions ranging from 12mm to 18mm, and whose feature size is five times (5X) the size of the printed feature on the wafer. For example, a 1μ feature, appears on the reticle as 5μ. The reticle is then stepped across the wafer 25 or more times, compared to once for full wafer lithography. This eliminates the yield problems associated with aligning a 1μ feature across a 150mm wafer, but it reduces the payload available for prototyping from 6000 sq. mm, to approximately 200 sq.mm. If we assume that the cost of a fabrication run is of the order of $75k, and that the users all submit projects of the same size, then the user's cost is as shown in the following table:

TECHNOLOGY	NUMBER OF USERS	COST/PROJECT
2.0μ (FWL)	75	$ 1,000
1.5μ (1X)	15	$ 5,000
1.2μ (5X)	5	$15,000

NOTE: FWL means Full Wafer Lithography.
1X means 1X Stepper Lithography
5X means 5X Stepper Lithography
The costs shown above are representative costs only. Project costs depend on the project area, as well as on packaging methods.

As can be seen from the table, the number of users is determined by the type of lithography employed. Note that 5X stepper technology is more expensive than FWL 2μ technology, because the reduced payload area limits the number of users to 5 per run. If reticle management systems are used, the cost per project for the 1.2um size could be further reduced to $7,500 or perhaps $5,000 each. Another possibility is the use of direct write on wafer (DWW) processes. Technical problems, however, exist in all these areas, but we are looking into different ways of overcoming them.

Vendor selection for any given technology was based on performance, yield, and availability at the time of initial selection. An additional factor is that a customer needs to have a certain "critical mass", ie, volume, to be attractive to a given fabricator. This critical mass or volume is very dependent upon existing economic conditions as well as

the type of business sought by the IC fabricator.

2.0 TECHNOLOGY ACCESS - INTERFACES

Another problem that faces the researcher, is the task of establishing vendor interfaces, to one or more vendors. For a large number of users, (assuming that funding is available to support a large number of dedicated fabrication runs), and that the IC fabricators are willing to deal with a multitude of users requiring only a small number of parts, it becomes a matter of a significant duplication of effort by each of the researchers. This process can be likened to a process of reinventing the wheel for each individual case. The interfaces required, are extensive. They range from correction factors needed by mask and wafer fabricators ("bloat and shrink" factors) applied to the as-drawn design geometry (to insure that the designer receives designs with the specified feature sizes) to the layers used for the different process steps and the required field polarity for the phototooling. In contrast to individual designer/fabricator interfaces, the broker does this once for each fabricator and/or technology and the details are then transparent to the designer, who is free to concentrate on the details of his own research rather than on the manufacturing details.

III. TECHNICAL RESULTS

PRIMARY FUNCTION

The primary function of the MOSIS IC Brokerage Service established by USC/ISI to meet the requirements of this contract was to provide access to cost effective, advanced technology fabrication for the research and educational communities. A set of *basic principles* was formulated in conjunction with the Defense Advanced Research Projects Agency during the subject contract to guide the operation of the Service. These are stated below.

1.0 BASIC PRINCIPLES OF MOSIS OPERATIONS

(1) Service research and educational institutions (MOSIS' primary customers).

Tiny Chips for NSF/DARPA Educational use.
PCB Service
Technology Files for Design Tools
Technologies for Advanced Designs
Project Management

(2) Serve as Neutral Third Party Between Designer and Fabricator

Independent yield and performance monitor
Provide stable monitoring of foundries to assist designers

(3) Provide consistent and uniform access to multiple technologies

Provide continuous introduction of new technology and services

Current Technologies:

Digital CMOS: 2, 1.5, 1.2, and 0.8μ;
Low noise Analog CMOS : 2 and 1.2μ
PCB's;
GaAs;

Expected Future Technologies:

BiCMOS;
5V/12V Analog CMOS:
MCM's;
SOI CMOS

(Photonic Devices)
(Micromechanical Devices)
These last two are in parenthesis because they were not officially approved by DARPA at the time of writing of this report.

(4) Lower Prototyping Costs Through Multi-Project Concept

Cost to user ~ Cost of run/Number of users
Full-wafer lithography for 2um feature sizes = 80 users/run.
1X Stepper lithography for 1.5μ feature sizes = 10-15 users/run
5X Stepper lithography for 1.2μ feature sizes = 5-10 users/run
5X Steppers with reticle management systems = 10 - 20 users/run

(5) Ensure High and Uniform Product Quality

Product quality monitored independently of the wafer fabricator's tests.
Parametric test structures, yield monitor circuits and statistical control charts
Defect density statistics maintained on all vendors.

(6) Provide Vendor Independence in Multiple Technologies

Possible through the use of generic, scalable design rules

CURRENT MOSIS TECHNOLOGIES AND FABRICATORS

TECHNOLOGY	***VENDORS***
2.0μCMOS	*VLSI Technology*
	Orbit
2.0μ CMOS (analog options)	*Orbit*
1.2μCMOS/BiCMOS (analog options)	*AMI*
1.6μ CMOS	*HP NID, AMI*
1.2μCMOS	*HP NID*
0.8μ CMOS	*HP NID*
1.2μ GaAs	*Vitesse*

(7) Introduce Experimental Technologies Rapidly and Economically

The marginal cost incurred by MOSIS in introducing GaAs technology was approximately $95K.

2.0 GENERAL METHODOLOGY

Designers submitted their projects using either electronic mail or magnetic media to the MOSIS Service of USC/ISI. The MOSIS Service collected and merged the separate designs into a single phototooling set. The projects were then included in regularly scheduled fabrication runs through U.S. commercial phototooling, wafer fabricators and device assembly houses. The Service provided U.S. researchers with access to multiple fabricators and multiple advanced technologies, while maintaining low prototype costs. The latter is accomplished through the use of shared project fabrication runs. Appendix 4 contains samples of the documentation required from the users of the MOSIS IC prototyping service. To minimize the access problem USC/ISI developed simple sets of forms that contained a uniform set of requirements for the different classes of users, such as DARPA Research, University classes, DoD contractors, etc.

3.0 SUMMARY OF RESULTS

3.1 ACCESS TO ADVANCED TECHNOLOGIES

(1) Provided access to advanced 3μ, 2μ, 1.6μ, and 1.2μ CMOS technology as they became commercially available to the prototyping service..
(2) Qualified a 0.75u CMOS Bulk digital process from Hewlett Packard. This provides slightly more than a 50% increase in speed over the previous 1u digital process. Our standard 31 stage ring oscillator operates at 120 Mhz in this technology, compared to 75Mhz in the 1u technology.
(3) Qualified and provided access.to a 1.2μ VLSI DCFL GaAs process.
(4) Qualified and provided access to a linear capacitor option for switched field capacitor designs, to be used with the standard HP CMOS34 (1.2μ) process.
(5) Generated and distributed several sets of CMOS scalable design rules for use by the design community. Appendix 1 contains a detailed set of the CMOS Scalable Rules and a one page summary of the rules.
(6) Generated and distributed sets of I/O pads for use by the design community.

3.2 NEW SERVICES

Developed and implemented a Net-List-to-Parts Service using the DoD developed 1.2u CMOSN cell library and the HP CMOS34 cell libraries. This service allows a designer to bypass the details of generating a layout to describe the design, and instead, submit the design in a high level description format.
Developed and implemented a design rule checking service for submitted projects. Previously, designs had been checked for valid syntax, not for violations of the geometrical design rules.
Provided a printed circuit board (PCB) service for the DARPA design community.

3.3 COST REDUCTION

Cost/gate for 1u technology has been reduced from $1.03 in GFY88, to $0.67 in FY92 (a 35% reduction). Another way of looking at this is as a reduction from $720/sqmm in FY88 to $470/sqmm in FY92.

The cost/gate discussed above, is the cost/gate for a single device for a prototype project, and does not include the total number of units shipped to the designer. Currently the Government costs for a 1.2μ project are $330/sq. mm of RETICLE area. The reason for using "gate cost" rather than cost per unit area, is to permit an effective cost comparison between different feature sizes and different technologies for circuit useable silicon. The assumption used to arrive at these costs, was that, using a standard cell design, a gate density of 700 "equivalent" gates/sq.mm (ie, simple NAND, NOR etc, not DFF or other large cells) could be obtained in the 1.2um technology. This gives a cost of $0.47/gate. A 2$\mu$ design, using the same assumptions, has a gate density of 250 gates/sqmm and a cost/gate of $0.12. On the other hand, when the term "cost/gate" is used in the literature, a reference is normally being made to costs that are amortized over the entire product buy. For example, an IC buy for a device with 10k gates purchased at a rate of 10k units per year for 4 years results in 4x10**8 gates for the duration. If the total cost of the buy is $1M, then the cost per gate is 0.25c/gate.

The figure used for gate density for a given feature size, is of course subject to the design style and the particular library used to implement the design. The table below, provides the values for simple cell (NAND, NOR, AND, etc) dimensions, gate densities, and costs for several different libraries:

LIBRARY	**Cell Width (μ)**	**Cell Height (μ)**	**Gate Density (gates/ sqmm)**	**Cost/ Gate ($/gate)**
CMOSN	18	150	370	0.89
HP-CMOS34 *(low power)*	17	68	865	0.38
HP-CMOS34 *(high speed)*	21	68	700	0.47
SCMOS	16	40	1615	0.20

If we consider more complex cells, CMOSN does not suffer as much in comparison with the HP high speed library. The ratios of CMOSN to HP areas for a DFFSR cell is 0.89, not the 2 to 2.5 ratios we see with the HP low power simple cells. These numbers make no allowances for wiring overhead.

The CMOSN library was designed by NSA as a conservative, very high speed library. NSA has reported that the CMOSN library works well up to 100 Mhz. SCMOS is a

scalable version of CMOSN, implemented by Insitute for Technology Development (ITD), and is used in the Lager tool set.

3.4 TECHNOLOGY TRANSFER

During the duration of this contract, USC/ISI transferred the IC prototyping run closing system developed initially for use by the MOSIS Service to the DoD for internal use. Known as RMOSIS, this system is in use to provide access to classified and rad-hard device fabricarion. USC/ISI also provided support for the transferred technology.

3.5 SIGNIFICANT USER PROJECTS

Among some of the most significant of the projects fabricated through the Service are:
(1) MOSAIC C from the DARPA sponsored California Institute of Technology's Submicron Systems Architecture Project. This project is for an experimental fine grained multicomputer, consisting of over one million transistors in a 10 x 10 mm chip fabricated with a feature size of one micron. (CMOS34 HP 1u process).
(2)Two-Phase Dynamic FET Logic, (TDFL) from UC Santa Barbara's DARPA sponsored program. This project consist of a self latching sequential logic family in GaAs, which operates from two non-overlapping clocks and a single one volt power supply. The power dissipation per gate is very low, corresponding to 88nW/Mhz which is significantly lower than static 5V CMOS (5 μW/Mhz), or BiCMOS (8μW/Mhz) for the load and fan-out.
(3)Decision Feedback Equalizer, from the DARPA sponsored UCLA project on Digital Receiver Microcells. This is a 60 Mbaud DFE chip for adaptive equalization in digital radio modems fabricated in 1u technology, and contains in excess of 60k transistors.
(4) A gas sensor and IR point source from NIST. This is a silicon micromachined device fabricated through a standard CMOS foundry.
(5)AuroraII, a GaAs microcomputer prototype chip from the University of Michigan, This project is a MIPS architecture based pipelined GaAs microprocessor, consisting of 160,000 transistors, small on-chip instruction cache, support for two-level memory hierarchy, 32x32 register file, 32-bit modified Ling adders, read and write buffers, and a full scan comprised of all registers. It implements the MIPS II instruction set architecture in VLSI GaAs direct coupled logic, (Technology: Vitesse H GaAs 3). Expected performance is 170 native MIPS.
(6) DatapathTechnology, from SPEC. A GaAs library development chip done by SPEC under contract to DARPA using the Vitesse H GaAs 3 process.
(7) MUSIC3, a test chip from the University of North Carolina that incorporates a 1-T DRAM design (a la Don Speck), single-phase clocked latches, an on-chip DtoA converter, and various other circuits that will be critical in forthcoming PixelFlow ASIC's. The chip not only is a test substrate for these functions, but, if fully functional, will be used to build an ultrasound imaging array. (Technology: HP CMOS34 (1μ))
(9)RN1B, from MIT. A low-Latency Crossbar 4x4 (dilation 2) routing chip described

in - Knight, T. F., Technologies for Low Latency Interconnection Switches, ACM Symposium on Parallel Algorithms and Architectures, June 1989, pp. 351-358. Also mentioned in - DeHon, Andre M., Knight, T. F., Minsky, Henry Q., Fault Tolerant Design for Multistage Routing Networks, MIT A.I. Memo 1125, April 1990.HP CMOS34 (1μ)

4.0 OPERATION OF THE MOSIS IC PROTOTYPING SERVICE

4.1 INTRODUCTION

The Information Sciences Institute of the University of Southern California operated the MOSIS silicon prototyping service for the duration of this contract. The MOSIS service provided fast turnaround fabrication of integrated circuits in prototype or small production quantities to over 100 DARPA and NSF sponsored organizations. A moderate number of DoD contractors also made use of the prototyping service for their research efforts The. MOSIS service subcontracted for IC fabrication with commercial firms and provided designers an interface to the semiconductor industry. Users submitted designs to MOSIS using either electronic mail or magnetic tapes and received packaged parts in a few weeks. Accessing the US semiconductor industry through the MOSIS service drastically reduced the risk, time, and cost of system development based on custom and semi-custom chips. MOSIS provided a single and relatively constant interface to an industry known for its multitude of different interfaces and rapid technological changes. The following sections will discuss the management of the functions performed by the MOSIS Service.

4.2 PROTOTYPING SERVICE ACCESS

Access to IC chip fabrication was provided through multiproject fabrication runs where designs from the research community were submitted in tape or via electronic mail, merged together at USC/ISI, and then fabricated through commercial fabrication houses. An accounting system was maintained to provide detailed information on the nature, composition and costs of the fabrication runs.

Four principal products resulted from this activity. The first was the access to the U.S. semiconductor industry for chips, packages, testing, printed circuit boards, and advanced packaging provided to the DARPA research community. The second was the methodology of procuring small volume prototype parts in an economical fashion. A third product was the access provided to Universities and other NSF sponsored institutions to a low cost prototyping service. The fourth product was the transfer of the run-closing technology developed under this program to the Department of Defense, for use in their own classified work.

During the four years covered by this report, the MOSIS Service of USC/ISI processed a total of 7,574 projects through 322 fabrication runs in eleven different technologies, ranging from 3μ NMOS, to 1.2μ GaAs. These projects came from (1) DARPA sponsored research organizations, (2) university class projects, from the DARPA/NSF sponsored university VLSI classes, and (3) from DoD contractors and other Government organizations. The average turn-around time achieved for all technologies accessed by the service decreased from 10.2 weeks in GFY88 to 8.3 weeks in GFY91. This turn-around time is the time from the scheduled closing of a fabrication run to the time projects are mailed back to the designers.

4.3 ORGANIZATIONAL STRUCTURE

The Information Sciences Institute is divided into separate Divisions, each of which is subdivided into separate Projects. The individual Divisions are responsible for the technical performance of specific contractual tasks, while functions such as accounting, procurement, legal functions, computer operations, etc. are provided to the operating divisions by the Institute and/or the University. The costs for each of these functions are shared by the divisions and are categorized under the heading of Common and O&M costs. The MOSIS Service is a Project within the Silicon Systems Division.

4.4 MOSIS OPERATIONS, GENERAL.

The MOSIS Service managed the data and logistics needed to allow designers to design and then convert their geometrical data into packaged parts. It utilized the commercial semiconductor industry for all manufacturing steps. Figure 1 depicts the flow of data into the MOSIS Service and the subsequent flow of masks, wafers, and data between the fabricators and users (designers) of the Service. Figure 2 depicts the MOSIS internal data and product flow.

Geometrical and design data from different designers was assembled into phototooling (mask) data specifically targeted towards various wafer fabricators. The designer's geometrical description of the chip being fabricated was accepted in one of several commonly used descriptive formats such as CALMA GDSII, MEBES, and CIF. Each fabrication line received masks exactly the way their own masks are prepared, and with the precise geometry needed to process wafers. This geometry typically consists of alignment marks, critical dimension marks, and the fabricator's process control monitors, allowing the fabricator to determine whether the process specifications have been met. The transformations of the designer's geometry are completely transparent to the device designer, who is then free to concentrate on the design itself, rather than on the mechanics of mask procurement. The merging together of a number of different designs on one mask set had the additional advantage of sharing the cost of fabrication among a number of users, the individual cost of the project being then a fraction of the total cost of a dedicated manufacturing run. Mask fabrication was obtained through commercial vendors having E-beam mask making equipment. The mask manufacturers were provided with tapes containing the pattern files and a control file known as a job deck which specified the location on each mask where the pattern file has to be written. The mask manufacturers simply loaded the tapes and turned on the equipment which was then completely controlled by the MOSIS written tapes.

Wafer fabrication was also obtained from commercial semiconductor manufacturers. Stability of manufacturing lines and processes as well as volume capacity for those products requiring volume production were the principal reasons for the selection by MOSIS of vendors to the commercial sector. Among the vendors used and/or evaluated were: National Semiconductor Corp., IMP , Hewlett Packard, VLSI Technology Inc, Orbit Semiconductor Corp, Gould AMI, Vitesse Semiconductor Corp., and UTMC. The wafers were purchased on the basis of the fabricator's wafer proces specifications, no special "tweaking" of the manufacturing processing was required from the manufacturer. The manufacturer's process specifications

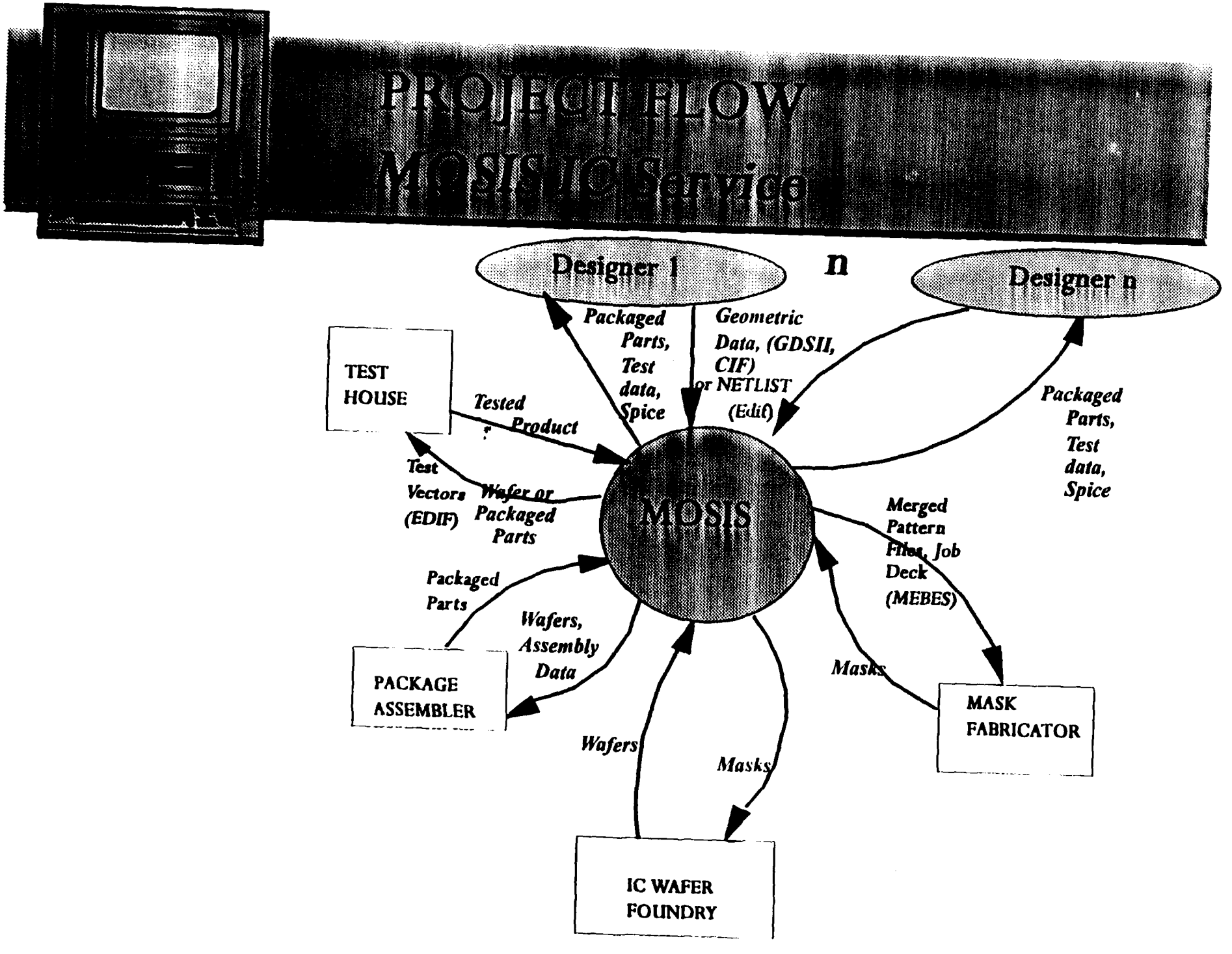

PROJECT FLOW
MOSIS Service
Designer 1
n
Designer n
Packaged Parts, Test data, Spice
Geometric Data, (GDSII, CIF) or NETLIST (Edif)
TEST HOUSE
Tested Product
Test Vectors (EDIF)
Wafer or Packaged Parts
MOSIS
Packaged Parts, Test data, Spice
Merged Pattern Files, Job Deck (MEBES)
Packaged Parts
Wafers, Assembly Data
PACKAGE ASSEMBLER
Masks
MASK FABRICATOR
Wafers
Masks
IC WAFER FOUNDRY

FIGURE 1

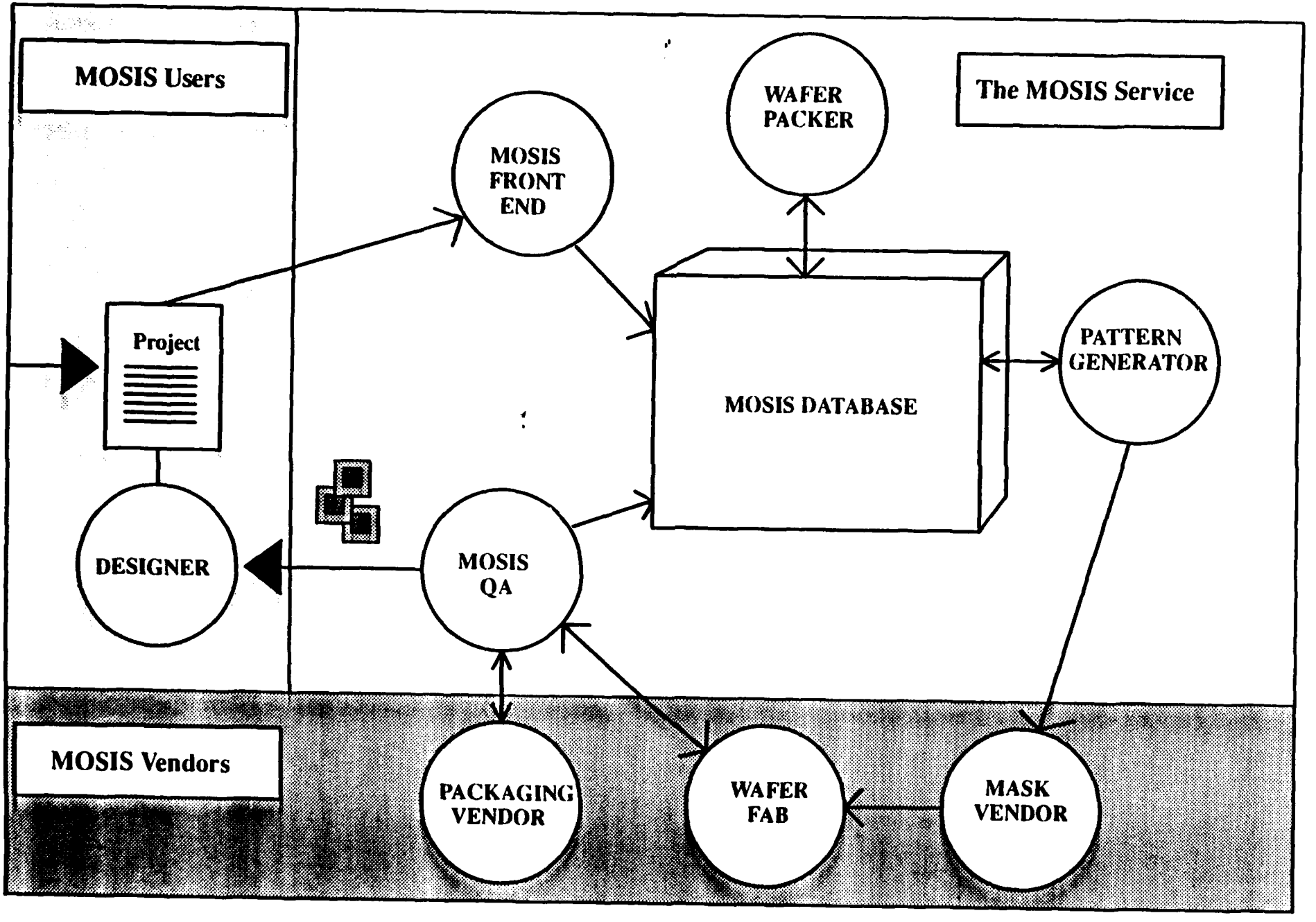

MOSIS Users
The MOSIS Service
WAFER PACKER
MOSIS FRONT END
Project
MOSIS DATABASE
PATTERN GENERATOR
DESIGNER
MOSIS QA
MOSIS Vendors
PACKAGING VENDOR
WAFER FAB
MASK VENDOR

FIGURE 2

form the basis for the acceptance of the wafers both at the semiconductor fabricator and later, at the MOSIS test facility.

4.5 VENDOR SELECTION

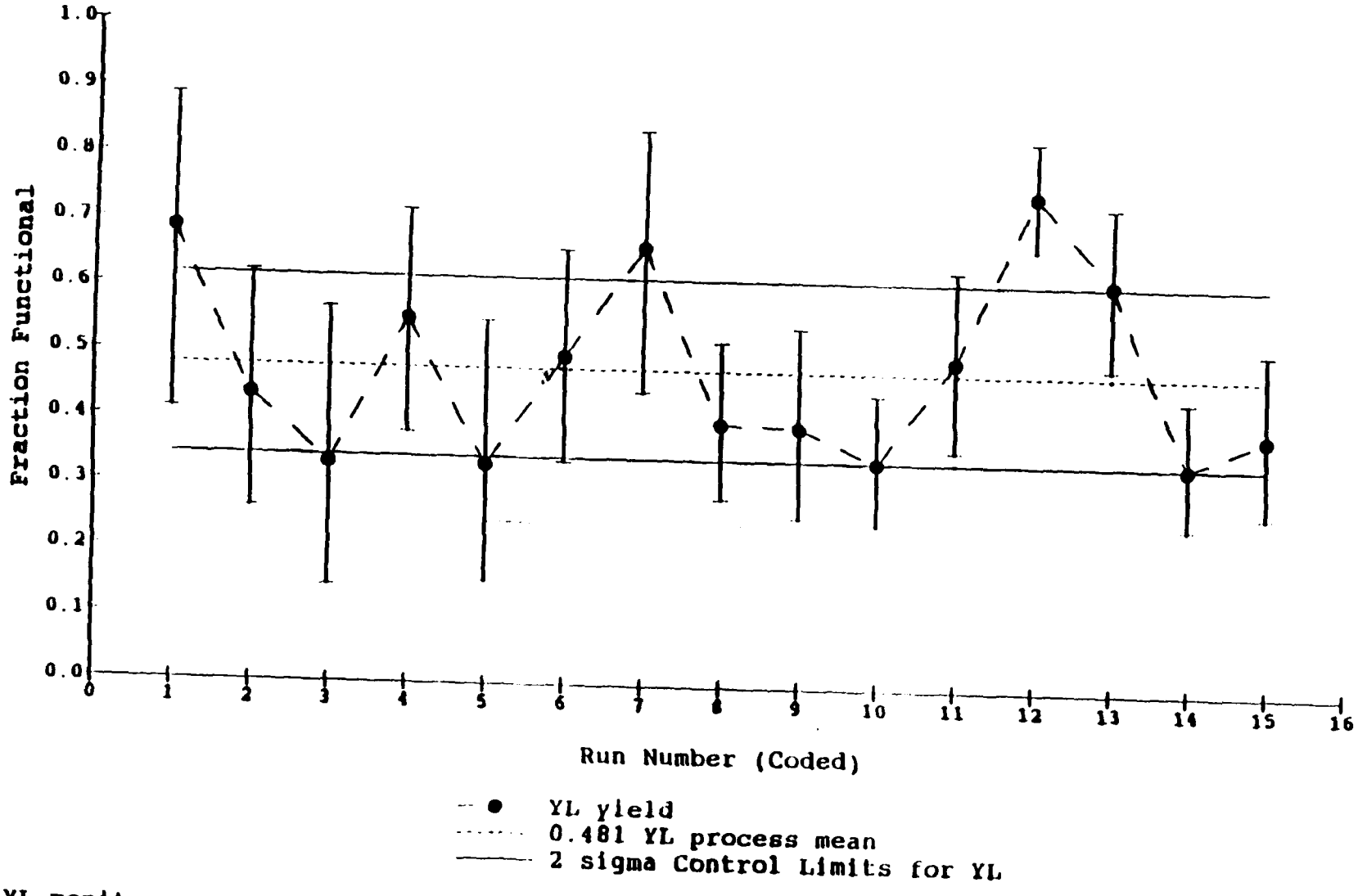
Vendors were selected on the basis of competitive bids, final selection was done only after evaluation test runs were completed. Requests for quotations were sent to fabricators which were initially selected on the basis of their technological capability in the areas of interest. These requests contained non-disclosure agreements, MOSIS wafer acceptance specifications, MOSIS geometrical design rules, etc. Upon receiving a response indicating vendor interest, the qualification process was started. The vendor's geometrical descriptions of their test structures, critical dimension figures, alignment marks, etc. were first obtained and these were then incorporated into the run-closing software. The next step involved the generation of test masks, incorporating both the wafer vendor's structures as well as the necessary MOSIS structures. Once these test masks were approved by both MOSIS and the wafer fabricator, a preliminary evaluation run was prepared containing an extensive number of test structures as well as some functional circuits of known behavior. Approval for regularly scheduled runs was given once the structures on the test run are successfully evaluated and DARPA's concurrence obtained.

4.6 FABRICATION RUN CONTROL

Submitted design layout files of projects, were screened by an automated check for valid syntax prior to being placed in the fabrication queue. Checks were made also for valid technology parameters, validity of account being charged, etc. before the project was assigned to a fabrication run. At the time a run is closed, all the information pertaining to the run was placed in a "RUN BOOK". This book is used by all the personnel involved in the processing of the particular run, and contains all the information generated during run processing. The information contained in the run book includes applicable work orders, mask inspection data, project bonding diagrams, wafer test data, etc. and serves as a complete history of the run. An operational manual describes the run closing process in detail.

4.7 PRODUCT ACCEPTANCE

Wafers received by MOSIS contained the manufacturer's process control monitors, as well as a set of MOSIS developed parametric test structures and yield monitors to measure the defect density of a particular run. Final acceptance of the finished wafers occurs at the MOSIS test facility using selected parametric tests performed on the individual wafers. The test results from each wafer are checked for compliance to the specification limits, and the best wafers were then selected for packaging. Although the yield monitors did not form a part of the formal acceptance specifications for wafers, they were used to monitor the quality of the incoming product from different manufacturers. Manufacturers whose products failed to provide satisfactory yields as measured by the yield monitor, were dropped from the list of approved vendors. In addition to the yield monitor, users' test reports are used to assess the quality of a particular fabrication run. Figure 3 is a sample of a MOSIS control chart for the information derived from the Yield Monitor. Appendix 2 contains a description of the



YL monitor area: 0.4546 cm^2
The error bars of YL represent 0.95 confidence bounds

FIGURE 3

MOSIS Process Monitor structures.

In addition to the process control and yield monitor structures , wafer level reliability test structures developed under a separate DARPA program, were used during the initial vendor qualification programs during the latter part of this contract.

Wafers meeting the electrical inspection criteria were visually inspected before being sent out for sawing and packaging. Commercial assembly houses were used for sawing and assembly into finished parts. All vendors used perform a visual die inspection before assembly and a package inspection after the assembly. To verify these results, MOSIS selected statistical samples from finished lots of parts and performed visual inspection for bond quality, and project identity verification. The sample is selected using the statistical tables provided in MIL STD 105.

4.8 ACCOUNTING PROCEDURES

In order to track customers and costs expended in fabrication runs, a comprehensive computerized accounting system was maintained which functioned in an almost completely automatic mode. The projects submitted were sized by the system upon submission, the area computed, and the cost of the project was then assessed against the customer's account.

5.0 TECHNOLOGY DESCRIPTIONS

5.1 IC FABRICATION TECHNOLOGIES ACCESSED BY MOSIS

The technologies that were made available through the MOSIS Service during the contract duration ranged from 3μ NMOS to 1.2μ GaAs devices. Even though a technology may be classified primarily by the type of construction (e.g. CMOS) and minimum feature size, there are a number of other significant features that have to be addressed when making the technology available for wide access. Process differences such as the number of layers of metal and/or polysilicon, or the number and type of wells (in CMOS) can also make a significant difference in the design styles and quality constraints. Most important, perhaps, is which vendors can make the particular technology available for access by the MOSIS Service. The early choice for CMOS technology employed P-Wells on an N-type substrate. This choice was made because with the level of fabrication technology available at the time, the N-type substrate was not inverted as readily as a P-type substrate by the alkali metals, such as sodium, a very common and hard to eliminate contaminant at the time. The inversion of the substrate would reult in a shunting path for the current from the well to the edge of the die. As the semiconductor processing techniques improved, eliminating the presence of alkali contaminants from processing areas, processes began to migrate towards the faster N-well technology.

5.1.1 IC TECHNOLOGY DESCRIPTIONS

See Appendix 5 for a summary of the current IC technologies supported by MOSIS and the key parameters for each of the technologies as well as available IC package characteristics.

3μ NMOS (NMOS3). One level metal and one level polysilicon. Projects for this technology designed using the MOSIS Scalable NMOS design rules, v.1, dated November 1984. These rules were based on the Mead-Conway design rules. Suppliers were VLSI Technology and Orbit Semiconductor.

3μ P-Well CMOS (DIGITAL) . Several versions of this technology were fabricated. The earliest versions had one level of metal and one of polysilicon or two levels of metal and one polysilicon level . Projects were designed using the MOSIS 3μ CMOS Design Rules, dated Nov. 1985. Later versions of this technology had one polysilicon and two metal levels and were designed using the MOSIS Scalable Design Rule Set, Rev 5, dated Nov. 1986. Vendors were VLSI Technology, Orbit, Hewlett-Packard,UTMC.

3μ P-Well CMOS (ANALOG). One version of this technology was fabricated, using one metal and two polysilicon layers. This technology was replaced by the 2μ feature size with two metal layers and two polysilicon layers. Vendor was Orbit Semiconductor.

2μ P-Well CMOS (DIGITAL). This was the earliest version of the 2μ technology made

available by the Service. All versions of this technology were fabricated with two levels of metal and one level of polysilicon. Vendors were UTMC, Orbit.

2μ P-Well CMOS (ANALOG). This technology was fabricated with two levels of polysilicon and two levels of metal. It continues in use. Vendor was Orbit.

2μ N-Well CMOS, (ANALOG) This technology was fabricated with two levels of polysilicon and two levels of metal as well as a limited set of bipolar options. It continues in use. Vendor was Orbit.

1.6μ N-Well CMOS (DIGITAL) . Two levels of metal and one of polysilicon. Earliest version of the high speed digital processes offered. Replaced by the 1.2μ CMOS34 process. Vendor was Hewlett-Packard.

1.2μ N-Well CMOS (DIGITAL). Two and three levels of metal and one of polysilicon with a linear capacitor option (for switched capacitor designs). Vendor was Hewlett-Packard.

0.8μ N-Well CMOS (DIGITAL). Two and three levels of metal and one of polysilicon. Vendor was Hewlett-Packard.

1.2μ GaAs. DCFL Logic. Vendor Vitesse.

PWB. The MOSIS Service supported a limited PWB brokerage service during the duration of this contract. Design formats were accepted from the users in Gerber format or as film. No board assembly was performed, only bare board fabrication was supported. Primary vendor was Multek.

A graph showing the volume vs time for the MOSIS service from its inception through the last *calendar* year for the different technologies accessed during that time is shown in Figure 4.

MOSIS PROTOTYPING VOLUME - CY81 THRU CY91

Year	Qty.
1981	281
1982	809
1983	1,322
1984	1,634
1985	1,790
1986	1,683
1987	1,396
1988	1,429
1989	1,880
1990	2,300
1991	2,259

TOTAL
16,783

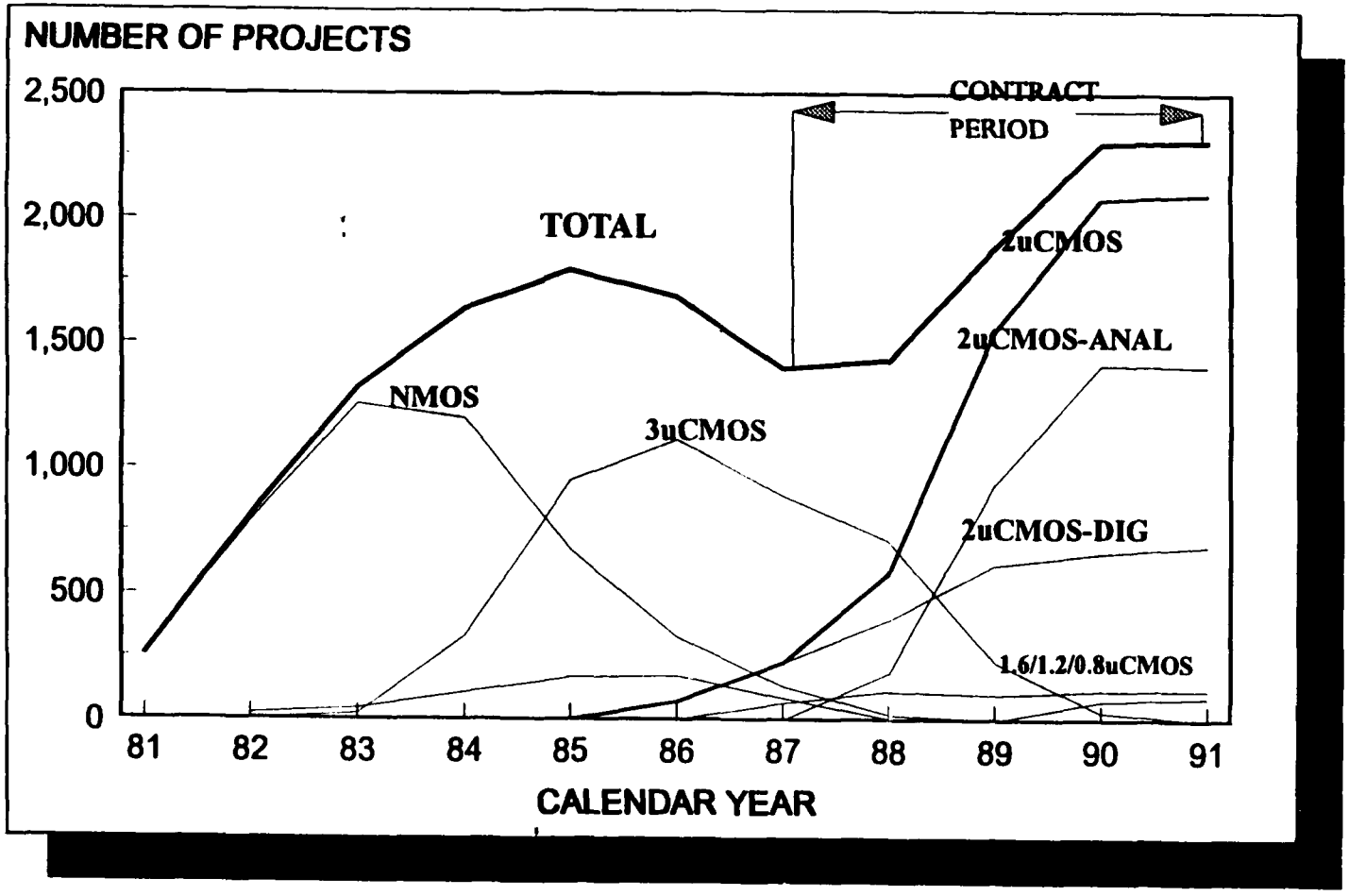


FIGURE 4

5.1.2 Chronology of MOSIS Implementation of Different Technologies

Note:Technologies available for which there was no demand are omitted from this table.

	Technology	Feature size	Metallization	New Packages
1981	NMOS,digital	5μ, 4μ, 3μ	1 layer	12DIP
1982	NMOS, digital	5μ,4μ,3μ	1 layer	40, 64 DIP
new	CMOS, digital	5μ	1 layer	
1983	NMOS,digital	4μ,3μ	1 layer	24 DIP; 84,128 PGA
	CMOS, digital	5μ	1 layer	
new	CMOS, analog	3μ	1 layer	
1984				
1985	NMOS,digital	4μ, 3μ,	1 layer	
new	CMOS, digital	3μ	2 layers	
	CMOS, analog	3μ	1 layer	
dev	CMOS-SOS (Silicon-on-sapphire)	3μ		
1986	NMOS, digital	4μ,3μ	1 layer	
	CMOS, digital	3μ	2 layers	
	CMOS, analog	3μ	1 layer	
	CMOS,digital	2μ	2 layers	
new	CMOS-SOS	3μ		
dev	Printed circuit boards			
1987	NMOS,digital	3μ	1 layer	
	CMOS, digital	3μ	2 layers	
	CMOS, analog	3μ	1 layer	12 PCBs
	Printed circuit boards			
new	CMOS, digital CMOS-SOS40	2μ,1.6μ	2 layers	
dev	Wafer Scale Int.	3μ		
new	Printed circuit boards			
1988	NMOS,digital	3μ	1 layer	28 ceramic DIP
	CMOS, digital	3μ	2 layers	
	CMOS,analog	3μ	1 layer	
	Printed circuit boards			
new	CMOS, digital	2μ,1.6μ	2 layers	
new	Wafer Scale Int.	3μ		
dev	CMOS, analog	2μ	2 layers	
dev	CMOS, digital	1.2μ	2 layers	

NMOS service discontinued by the end of 1988 for lack of demand.

1989	CMOS, digital	3μ	2 layers	84, 108 ceramic PGA
	CMOS. analog	3μ	1 layer	User DIP,PGA, LCC,
	CMOS,digital	2μ,1.6μ,1.2μ	2 layers	
	Printed circuit boards			
new	CMOS,analog	2μ	2 layers	
	Wafer Scale Int.	3μ		
dev	Wafer Scale Int.	2μ		
dev	CMOS,analog with bipolar options	2μ	2 layers	
dev	GaAs	1.2μ	3	
1990	CMOS, digital	3μ	2 layers	84,108 ceramic PGA
	CMOS,digital	2μ,1.6μ,1.2μ	2 layers	
	CMOS,analog	2μ	2 layers	
	Wafer Scale Int.	2μ		
	Printed circuit boards			
new	CMOS,analog with bipolar options	2μ	2 layers	
new	GaAs	1.2μ	3	

3μ CMOS discontinued after 4-11-90 for lack of demand.

1991	CMOS,digital	2μ,1.6μ,1.2μ	2 layers	
	CMOS,analog	2μ	2 layers	
	CMOS,analog with bipolar options	2μ	2 layers	
	GaAs	1.2μ	3	
	Printed circuit boards			

5.1.3 Chronology of MOSIS Service Enhancements

1980

- - ISI conducts first trial run for 65 nMOS projects by 8 users, with good results.
-- Creates, offers users VLSI Design Library with some basic circuits for bonding pads, shift registers, etc., acquired from Xerox PARC.
-- Work toward CMOS implementation capability begins.

1981

-- ISI offered first "official" MOSIS chip fab run, accepting requests by ARPANET and Telenet, accepting CIF 2.0 format, with NMOS 3, 4, & 5μ feature sizes and one layer of metallization.

1982

-- NSF-DARPA cooperative agreement provides cost-free access to MOSIS services by U.S. universities and colleges approved by NSF for projects serving educational purposes, for graduate and undergraduate courses, and principal investigator projects supported by NSF.

1983

-- First CMOS runs; establishes MOSIS design rules
-- Packaging options expanded from two to five. Plans to offer 1.25 features in 1983 were frustrated, and ultimately delayed until 1988.
-- CSNet was added to the accepted communication services.

1984

-- Adds Printed Circuit Board fab to its services.
-- Adds NSA design rules for CMOS implementation
-- CALMA GDS2 stream added to CIF as design geometry submission format
-- MILNET added to the accepted communication services.
-- To improve defect screening and yields, MOSIS/Stanford begin to develop functional test language (STEVE).
-- Offers standard pad configurations to facilitate wire bonding of devices
-- Offers on-line access to its library of common circuits, I-O pad circuits, etc.
-- Experimental runs of 1.2μ CMOS.
-- Turnaround 4 to 13 weeks depending on technology involved (nMOS shortest)

1985

-- Accepts fabricators rules for CMOS, in addition to MOSIS & NSA rules
-- Begins to accept MEBES geometry formats in addition to CIF &CALMA.
-- User library expanded to include standard logic and computational functions and memories: USG 3μ p-well CMOS/Bulk standard cell library available

-- MAGIC technology file for scalable CMOS designs from UCB on-line
-- Additional quality assurance efforts; further experiments w/ 1.2μ CMOS, with intent to offer by end- 1986.
-- Prototype 1.25μ fabrication started, with GE and Hughes acting as foundries.

1986
-- Experimentation begun on GaAs, wafer-scale integration,
-- Formal wafer acceptance spec negotiated with all vendors.
-- Two vendors qualified for 1.2μ CMOS/bulk. 1.6μ CMOS available.
-- **new** parametric test structure (SUPERCHARGER) & report generator in use.
-- Technology Transfer MOSIS technology transferred to NSA for classified fast-turnaround facility.
-- "Tiny chips" program. using standard pad frame to permit automated bonding, offers 4 chips for $400 at 3μ; aimed at needs of university classes. A Tiny Chip is a means of making custom chips available to designers at a very low cost. By being able to put a large number of different designs on one run, and requiring a predefined pad frame, which permitted packagers to use automated bonding equipment, μhe cost per device was Greatly reduced.

1988
-- 2μ Tiny chip added
-- First 1.2μ CMOS/bulk standard runs commence
-- Vendor-independent DoD CMOSN standard cell library available for 2μ and 1.2μ design; VTI 2μ library also available
-- SPICE Level 2 and SPICE BSIM parameter measurements available to upgrade the quality of monitoring

1989
-- First experimental prototyping run in GaAs
-- Ultratech stepper lithography (1.5μ) and 5x stepper lithography (1.μ1.5μ) implemented
-- First 1.2μ project runs
-- 2μ CMOS 2M with double poly (low-noise analog) commences
-- NPN bipolar technology available;
-- Special analog design options made available through commercial vendors
-- MOSIS library offers DoD standard cell library accepted by all MOSIS vendors, incorporated into five commercial design tool sets

-- MOSIS begins "netlist-to-parts" service permitting users to specify standard cells from commercial DoD sources for inclusion in design by MOSIS
-- MOSIS exploring gate array and EEPROM offerings might be feasible

1990
- - Last 3μ CMOS run scheduled
-- GaAs runs to be offered on "demand" basis in 1991
-- Design kits available from commercial standard cell library suppliers for both CAE and CAD tools

-- Experimental runs at 0.8μ 3M planned for Fall, to be available mid- 1991
-- Acceptability of commercial 1.6μ BiCMOS offerings being assessed
-- Tape automated bonding for 1μ processes being evaluated

5.2 COMPARISON OF PHOTOLITHOGRAPHIC PROCESSES

Advanced IC technologies use photolithographic processes to define the features of the circuits during fabrication. Typically, feature sizes larger than or equal to 2μ can use full wafer lithography processes. In these processes, the feature size on the mask is the same size as the feature size on the finished wafer (1X process). Due to the difficulty of maintaining dimensional and alignment control over a wafer of 125-150mm dimension for micron sized features, manufacturers have shifted to stepper based technology for dimensions smaller than 2μ. Two types of steppers are in common use: 5X and 1X Ultratech. The 5X steppers find use in all technologies below 2μ, whereas the 1X Ultratech steppers find use in the range between 1.2μ and 2μ. The 1X Ultratech steppers are better suited for prototyping purposes, since the available payload is 900 sq.mm (three fields, each one 10x30mm), compared to 200 sqmm (one field, 14x14mm) for a typical 5X process. This means that all other things being equal, the cost (not including the masks) for projects should be less by a factor of four when using 1X steppers than 5X. In reality, once the mask costs are taken into account, the price differential is between 2 and 3 times. As dimensions decrease below 1μ, yields and performance favor the 5X process. This is shown in the comparison table below:

Consider a 16M DRAM, with a 0.5μ feature size.

CHARACTERISTIC	1X Ultratech	5X Reticle
Min. mask feature size (μ)	0.5	2.5
Registration Accuracy (nm)	16	83
Defect Size Limit (nm)	<70	<350
Surface Flatness (μ)	<0.3	<1.5
Pellicle Particle Limit (nm)	70	350

Since the mask feature sizes are 5x larger for the 5X reticle, the defects that can be tolerated on the mask are also 5x larger, resulting in a much more tolerant process and higher yields. Unfortunately, the reduction in payload available for a prototyping run (where only a small number of parts is desired), results in higher project costs. When compared with a full wafer lithography run, having a payload of 4500 to 6000 sqmm, the difference is even more significant.

5.3 YIELD COMPARISONS

5.3.1 YIELD MODELS

During the operation of the MOSIS Service, several yield models (Poisson, Seeds, and Murphy's models) were evaluated for the purposes of providing users with information they could use to estimate the number of acceptable parts they could obtain from a particular process. The yield models were also necessary to provide comparisons between the different manufacturers and to provide data that designers could use to determine if their results were what was expected for the given manufacturer and their chip size. All of the models depend directly on the project area. All other things being equal, the larger the project, the lower the yield for a given process.

POISSON:
This is the simplest model and assumes a uniform distribution of point defects, i.e., a constant defect density over both wafer area and from wafer to wafer. It tends, however, to underestimate the yield of larger chips. For this reason, this model was discarded early in the evaluations.

$$Y = \exp(-\lambda A)$$

where

Y = *yield*
A = *area of chip*
λ = *defect density*

SEEDS:
Assumes a variable defect density, and in addition, that the probability of having a large defect density is low, and the probability of having a small defect density is high. This model did not provide as good results as Murphy's model and was not used routinely. It has been found accceptable in predicting yields of large chips in well established, low defect density processes.

$$Y = \exp(-\sqrt{\lambda A})$$

where

Y = *yield*
λ = *defect density*
A = *Area*

MURPHY:

This model assumes that the defect density is Gaussian, with the lowest value at the center of the wafer. The model showed a good correlation with observed results on both large and small chips. Consequently, it was used consistently for yield estimates.

$$Y = \left(\frac{1 - \exp(-\lambda A)}{\lambda A}\right)^2$$

where

Y = *yield*
λ = *defect density*
A = *area of chip*

Figure 5 shows the expected IC yield from vendors accessed by the MOSIS Service for different project sizes. As depicted in the figure, the vendors fall into two groups with different process defect densities.

5.3.2 RESULTS - MOSIS PERFORMANCE STATISTICS BY GOVERNMENT FISCAL YEAR FOR THE CONTRACT DURATION

YEAR	GFY88		GFY89		GFY90		GFY91	
TECHNOLOGY	Number of Runs	Ave. Number of Proj.	Number of Runs	Ave. Number of Proj.	Number of Runs	Ave Number of Proj.	Number of Runs	Ave. Number of Proj.
3μNMOS	1	20						
3μPW Dig	17	45.1	9	34.3	3	15.7	1	1
3μPW AnaL	2	7	1	1	0	0	0	0
2μPW Dig	9	19.2	0	0	0	0	0	0
2μPW AnaL	2	30.5	14	48.9	14	78.6	19	77.2
2μNW Dig	11	16.8	13	42.2	13	55.7	15	40.7
2μNW Anal	0	0	2	86.5	5	42.6	6	56.2
1.6μ Dig	22	3.9	10	5.9	6	7.7	2	18
1.2μ Dig	4	13.5	6	6.2	10	5.6	17	6.8
0.8μ Dig	0	0	0	0	0	0		
GaAs	0	0	2	7	2	15	4	11.5
Wafer Scale	0	0	1	1	3	11.3	1	1
PCB	20		17		22		20	
YR TOTALS	88		75	32.5	78	232.2	85	37.7
4YR TOTAL							326	42.8

5.3.3 Technologies Facilitated by the MOSIS Service

Computer-Aided Design & Graphics Tools
-- CAESAR: UCB, John Ousterhout,
-- MAGIC Ousterhout, UCB; (Valid, Viewlogic, Mentor, Daisy, Cadence) 1979-82
-- Geometry Engine, Stanford, Jim Clark (Silicon Graphics, Inc.)
-- PIXEL: general purpose experimental graphics engine under PIXEL Planes Project at UNC; capabilities
-- SPICE, UCB

Automation Technology Program, circuit simulator (design verification tool)
-- MOSSIM, UCB Automation Technology Program, switch simulator (design verification tool)
General RISC Architectures
-- RISC I & RISC II: (SPARC
-- SUN Microsystems)
-- MIPS & MIPS-X, Stanford, John Hennessy, (Microprocessor without Interlock between Pipe Stages) (MIPSCO.)

Systolic Array Architectures
-- LINK, CMU systolic array chip.
-- WARP, CMU, H.T. Kung, (iWARP) INTEL Symbolic Processing Architectures
-- The Syracuse AI coprocessor
-- SOAR, UCB, Patterson
-- SPUR, UCB. (Symbolic processing using RISC and multiprocessors)

Neural Networks
-- Cochlea, Retina (neural network analog chips) Caltech (Synaptics, Inc.)

Parallel Processing Architectures
-- The Connection Machine, .μT
-- The Tree Machine, Caltech -
-- Non-Von, Columbia s Tree Machine architecture 1984
-- Hypercube / Cosmic Cube, Caltech, Charles Seitz
-- Monarch, Bolt Baranek & Newman (BBN), Medium Scale Prototype of a large-scale tightly coupled butterfly parallel processor developed as part of DARPA's Strategic Computing Initiative.
-- MOSAIC: Caltech's homogeneous multiprocessor architecture

Routing.

Message-Passing Devices

-- Torus Routing Chip (Wormhole routing and virtual channels)
-- MOSAICA (fine-grain message-passing system in NMOS
-- MOSAICC (fine-grain message passing system in CMOS): INTEL
-- CRRES (Jet Propulsion Lab) (MOSFET matrix for transistor parameter extraction, sampler for propagation delay measurement. 1984
-- Digital Orrery, SIMD message-passing system for orbital computations Other Specialized Comμonents μAnalog-to-Digital Converters)
-- Algorithmic monolithic CMOS A/D converters, UC-B, Paul Grey; incorporated into several commercial products including a single-chip data acquisition system by Microlinear Corp.
-- High-speed pipelined AID converters, UC-B, Paul Grey, which will allow economic implementation of an AD/D interface directly on video signal processing chips. Fabrication
-- WSI - Wafer Scale Integration, Lincoln Laboratory, supported by DARPA as part of its VLSI program, fabricated at least eighteen projects on MOSIS;
-- SOAR

Other

-- The Quarter Horse
RMOSIS
--1986: The National Security Agency established its own "clone" of the MOSIS system for prototyping classified chip designs using MOSIS techniques for fast turnaround.

5.3.3 RESULTS - TECHNOLOGY COMPARISONS

This section summarizes the results obtained from different technologies during the performance of the contract. The information is presented as a series of graphs.

Figure

(1) Graphs of variation of defect densities with manufacturers
(2) RO frequencies vs channel length
(3) Reliability evaluations
(4) Chart of expected yield for different defect densities
(5) Expected yield from small samples

6.0 APPENDICES

The following appendices provide greater detail for selected topics associated with the operation of the MOSIS Brokerage Service. A summary of the information contained in the appendices is given below.

APPENDIX I

This appendix contains a complete set of the MOSIS Scalable and Generic CMOS Design Rules, Rev 6, Feb. 1988. Adherence to this set of rules guarantees working devices with the approved set of MOSIS fabricators as long as the design is correct. Also included in this Appendix, are one page summaries of the:

(1) "MOSIS 3μ PWELL CMOS BULK RULES", Rev 2
(2) "MOSIS CMOS SCALABLE RULES", Rev. 5
(3) "MOSIS CMOS SCALABLE RULES", Rev. 6

The first two, are earlier versions of the present set of rules, and are included to demonstrate the evolution of the rule sets.

APPENDIX II

This includes a complete description of the 3μ and 2μ Tiny Chip Die Sizes. The 3μ size was the first one made available to the community, but was discontinued with the phasing out of the 3μ fabrication runs. These chips are important because they provide a low cost vehicle for the teaching of VLSI design courses at universities. They are also very useful for providing low cost verification of portions of circuit designs, prior to submitting a full size design.

APPENDIX III

This appendix contains samples of the forms and documentation used to access and work with the MOSIS Service. Included are:
(1) Basic Steps (for access).
(2) Project submission forms
(3) Documentation List
(4) Price List and Order Form
(5) Customer Agreement Form
(6) Application for Access to Support Research and Government Agencies
(7) Application for Access to Support Education

APPENDIX IV

The "MOSIS TECHNOLOGY SHEET" Provides a summary description of the available technologies provided to users of the service. Two graphs provide measures for the performance of devices fabricated with the technologies accessed by MOSIS. A 31 stage ring oscillator is included with every MOSIS fabrication run, fabricated with the CMOS Scalable Rules descibed in Appendix I. Measurements of this ring oscillator provided the performance data depicted in the two graphs.

APPENDIX V

This appendix contains a description of the CMOSN DoD developed cell library.

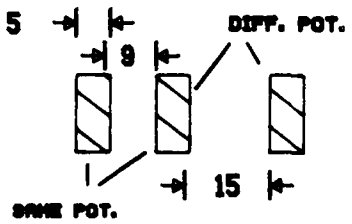
APPENDIX VI

"MOSIS PROCESS MONITOR" Description, dated April, 1989. This is the version currently in use. The process monitor is used to assess the quality of incoming wafer lots. The information is used as the basis of lot acceptance and wafer selection and is also used to extract SPICE simulation parameters provided to the users from every manufacturing run.

MOSIS 3 MICRON P WELL CMOS BULK

REVISION 2

P WELL



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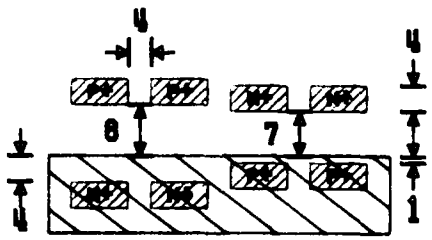
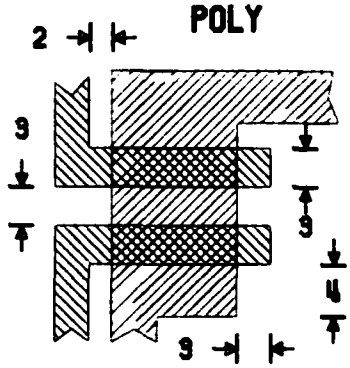
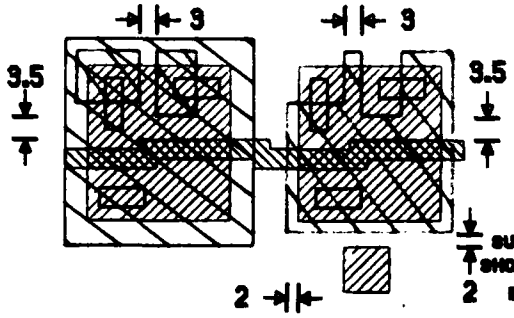


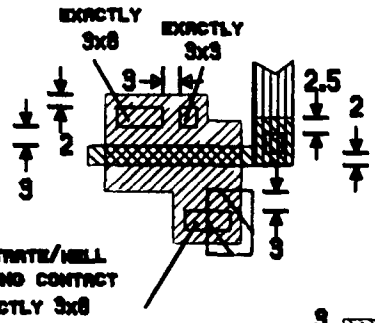
POLY



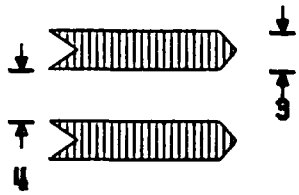
P+ SELECT



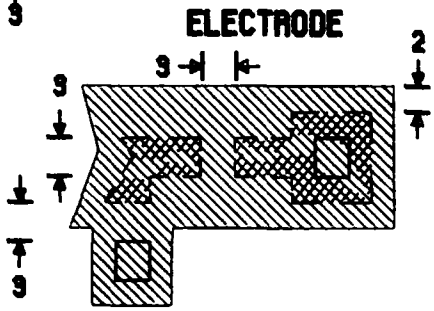
CONTACT



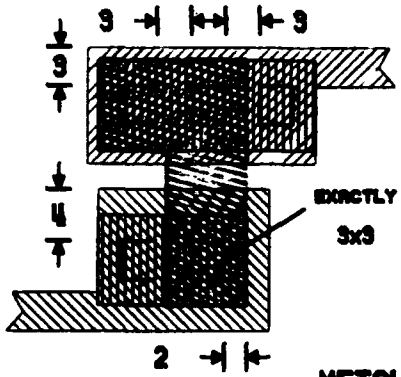
METAL1



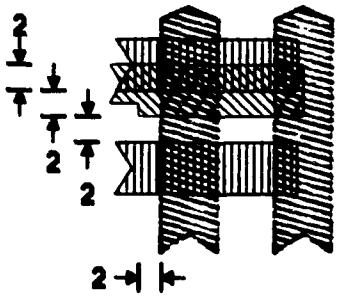
ELECTRODE



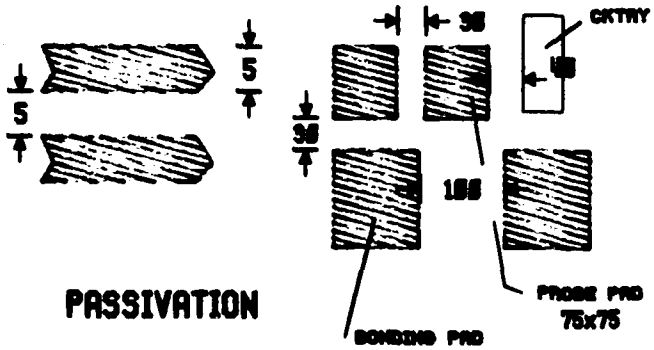
VIA



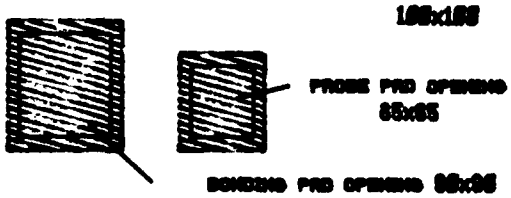
METAL2 CROSSING METAL1 AND POLY



METAL2



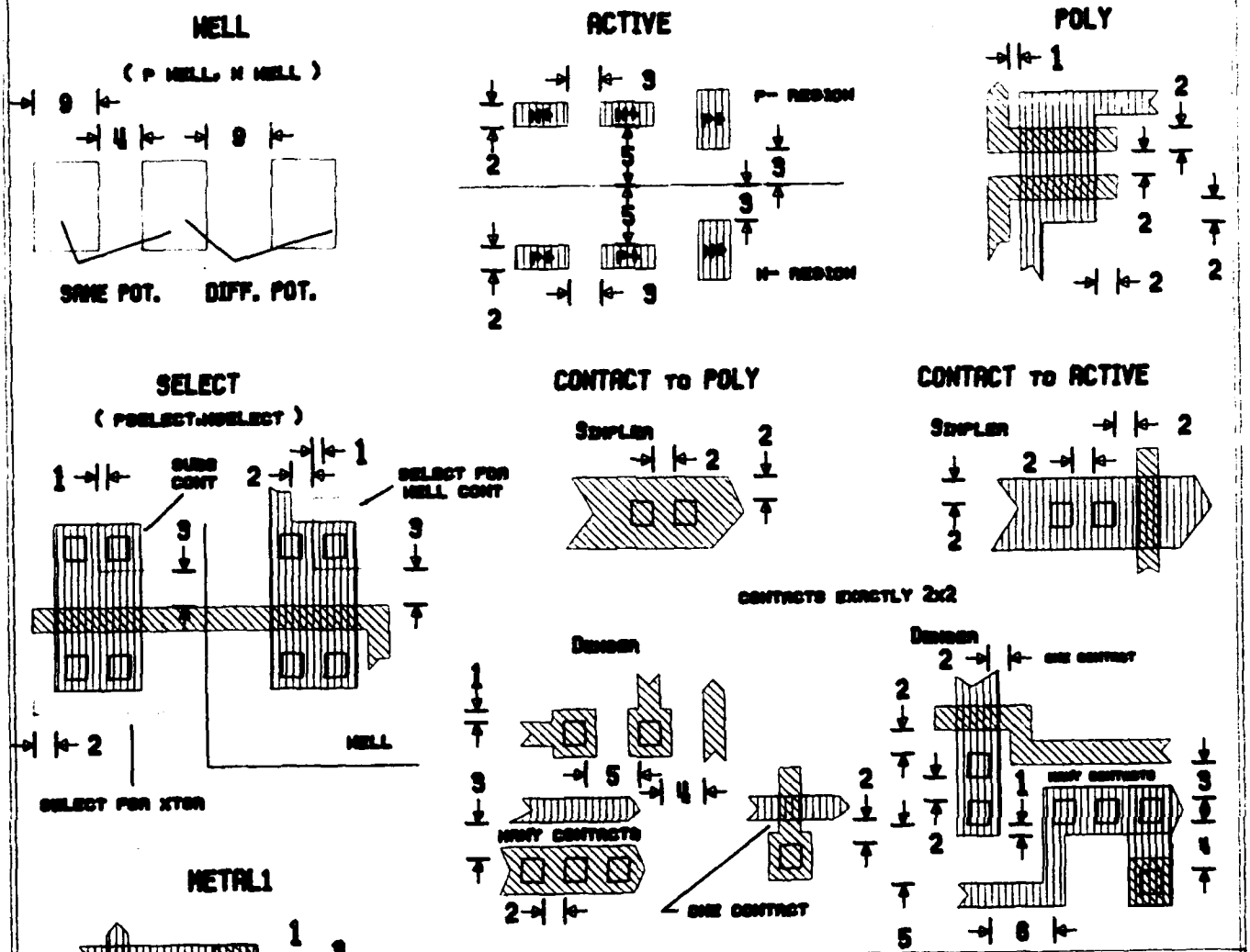
PASSIVATION



LAYER	CIF	CALMA #	COLOR
P-WELL	CW	1	
ACTIVE	CD	3	
POLY	CP	4	
P+ SELECT	CS	5	
CONTACT	CC	7	
METAL1	CM	8	
VIA	CV	13	
METAL2	CQ	14	
GLASS	CG	9	
ELECTRODE	CE	15	

NOTE: MOSIS DERIVES N+ SELECT MASK FROM P+ SELECT LAYER

MOSIS CMOS SCALABLE RULES (REV5)



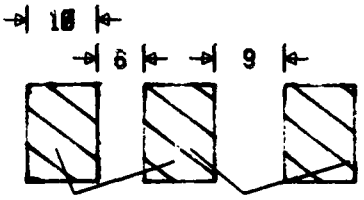
LAYER	CIF	CALMA #	COLOR
WELL	CWG	53	
PWELL	CWP	41	
NWELL	CWN	42	
ACTIVE	CAA	43	
SELECT	CSG	54	
PSELECT	CSP	44	
NSELECT	CSN	45	
POLY	CPG	46	
CONT TO POLY	CCP	47	
CONT TO ACT	CCA	48	
METAL1	CMF	49	
VIA	CVA	50	
METAL2	CMS	51	
OVERGLASS	COG	52	

ALL LAYERS MUST BE ON LAMBDA GRID EXCEPT
METALS WHICH CAN BE ON HALF LAMBDA GRID

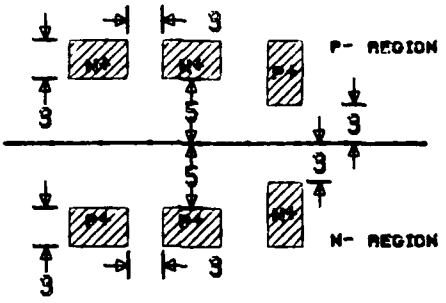
MUSIS CMOS SCALABLE RULES (REV6)

WELL

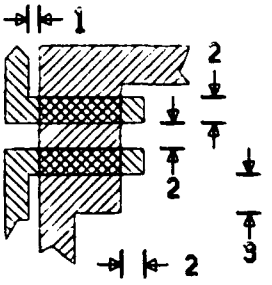
(P WELL, N WELL)



ACTIVE

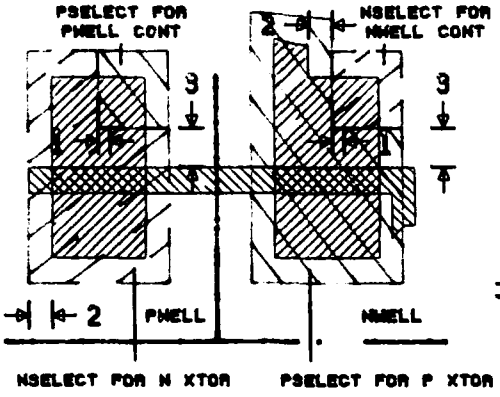


POLY

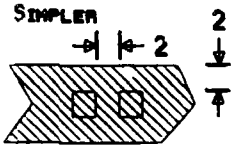


SELECT

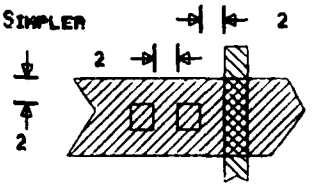
(PSELECT,NSELECT)



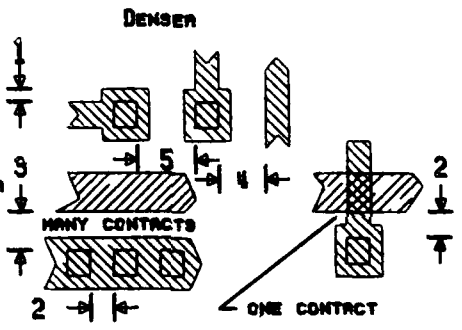
CONTACT TO POLY

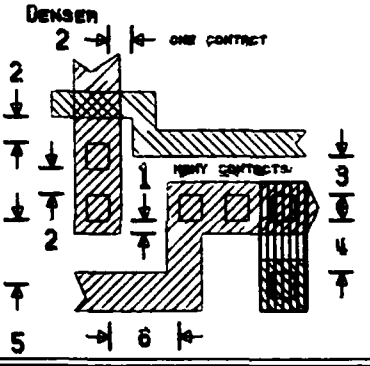


CONTACT TO ACTIVE

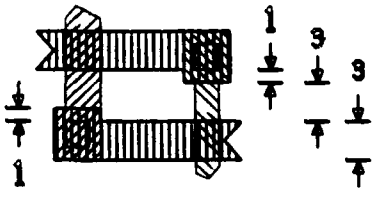


CONTACTS EXACTLY 2x2

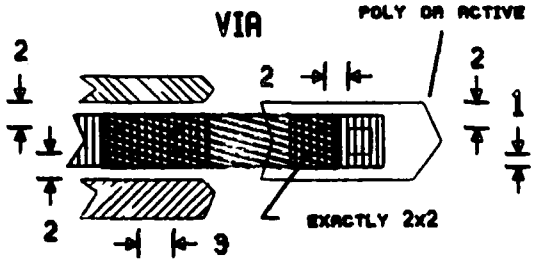




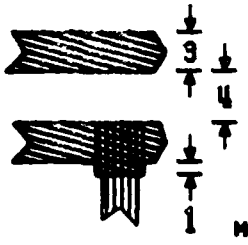
METAL1



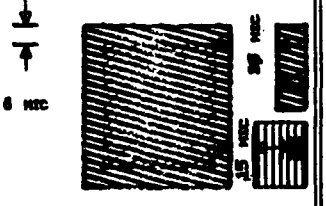
VIA



METAL2



OVERGLASS



PROBE PAD 75x75 MIC
BONDING PAD 100x100 MIC
MET2 REQD UNDR OVERGLASS

LAYER	CIF	GDS	COLOR
WELL	CWG	53	
PWELL	CWP	41	
NWELL	CWN	42	
ACTIVE	CAA	43	
SELECT	CSG	54	
PSELECT	CSP	44	
NSELECT	CSN	45	
POLY	CPG	46	
CONT TO POLY	CCP	47	
CONT TO ACT	CCA	48	
METAL1	CMF	49	
VIA	CVA	50	
METAL2	CMS	51	
CONT TO ELEC	CCE	55	
ELECTRODE	CEL	56	
OVERGLASS	COG	52	

ALL EDGES MUST BE ON HALF LAMBDA GRID

MOSIS

SCALABLE & GENERIC

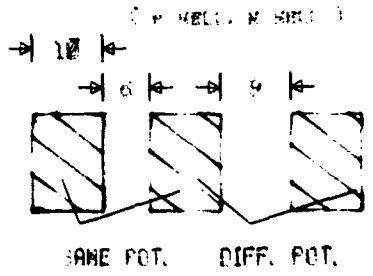
CMOS

DESIGN RULES

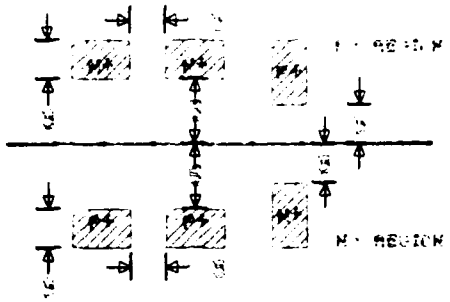
February 1988
Revision 6

MOSIS CMOS SCALABLE RULES (REV

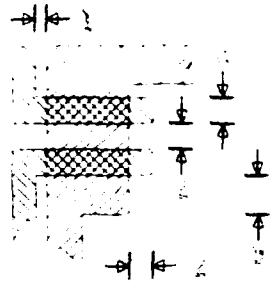
WELL



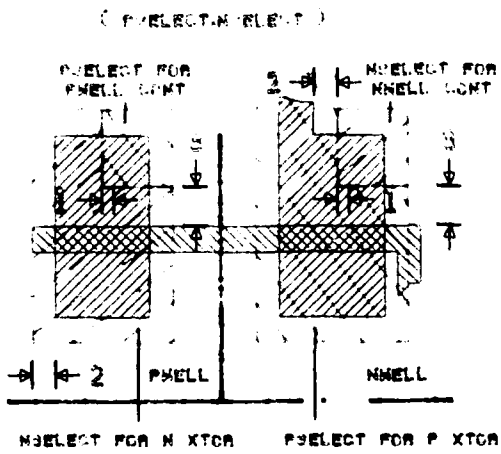
ACTIVE



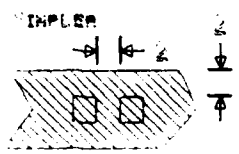
POLY



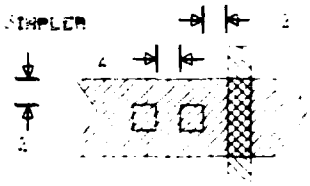
SELECT



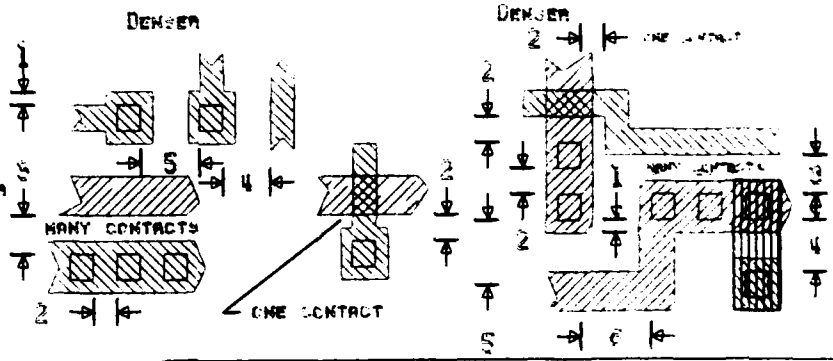
CONTACT to POLY



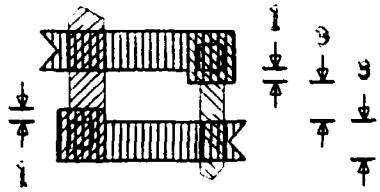
CONTACT to ACTIVE



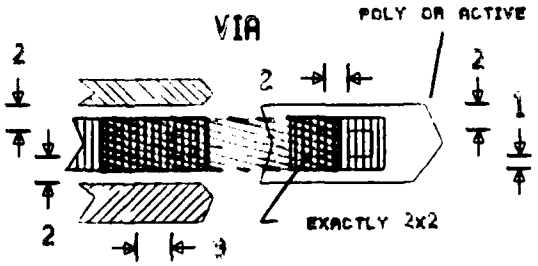
CONTACT EXACTLY 4x2



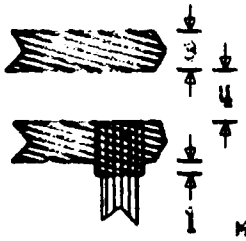
METAL1



VIA



METAL2



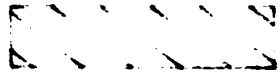
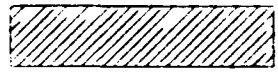
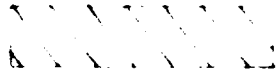
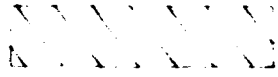
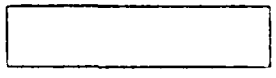
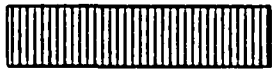
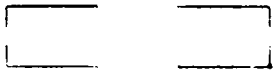
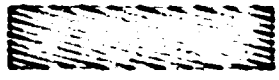
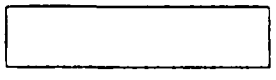
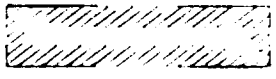
OVERGLASS

PROBE PAD 75x75 MIC
BONDING PAD 100x100 MIC
MET2 REQD UNDR OVERGLASS

LAYER	CIF	GDS	COLOR
WELL	CWG	43	
PWELL	CWP	44	
NWELL	CWN	42	
ACTIVE	CAA	43	
SELECT	CSG	34	
PSELECT	CSP	44	
NSELECT	CSN	45	
POLY	CPG	46	
CONT to POLY	CCP	47	
CONT to ACT	CCA	48	
METAL1	CMF	49	
VIA	CVA	50	
METAL2	CMS	51	
CONT to ELEC	CCE	55	
ELECTRODE	CEL	56	
OVERGLASS	COG	52	

ALL EDGES MUST BE ON HALF LAMBDA GRID

LAYER NAMES AND COLORS

LAYER	CIF	GDS	COLOR
WELL	CWG	53	
PWELL	CWP	41	
NWELL	CWN	42	
ACTIVE	CAA	43	
SELECT	CSG	54	
PSELECT	CSP	44	
NSELECT	CSN	45	
POLY	CPG	46	
CONT to POLY	CCP	47	
CONT to ACT	CCA	48	
METAL1	CMF	49	
VIA	CVA	50	
METAL2	CMS	51	
CONT to ELEC	CCE	55	
ELECTRODE	CEL	56	
OVERGLASS	COG	52	

TECHNOLOGIES AND REQUIRED LAYERS

PROCESS	TECHNOLOGY	REQUIRED LAYERS
PWELL AND N SUBS TWIN TUB	SCP	CWP CSN, CSP
N WELL AND P SUBS TWIN TUB	SCN	CWN, CSN, CSP
ALL *	SCG	CWG, CSG
ALL **	SCE	CWP, CWN CSP, CSN

* FOR A P WELL OR N SUBS TWIN TUB PROCESS,
MOSIS SETS CWP=CWG AND CSP=CSG

FOR AN NWELL OR P SUBS TWIN TUB PROCESS,
MOSIS SETS CWN=CWG AND CSN=CSG

** FOR A P WELL OR N SUBS TWIN TUB PROCESS,
MOSIS IGNORES CWN

FOR AN NWELL OR P SUBS TWIN TUB PROCESS,
MOSIS IGNORES CWP

INSTRUCTIONS FOR DESIGNERS

DRAW IN UNITS OF LAMBDA.

ON ANY LAYER NO SPACE OR FEATURE SIZE
MAY BE LESS THAN 2 LAMBDA WIDE.

ALL FEATURE EDGES
MUST BE ON A HALF LAMBDA GRID.

WHAT YOU DRAW WILL BE VERY
CLOSE TO WHAT YOU GET. MOSIS
WILL TELL YOU THE DIFFERENCES.

SCALE YOUR CIF OR GDS TO
METRIC UNITS. NEVER SUBMIT
A DESIGN IN CENTILAMBDA.

WHAT VALUES LAMBDA ?

LAMBDA=1.Ø MICRONS

FOR 2.Ø MICRON FABRICATORS

LAMBDA=Ø.8 MICRONS

FOR 1.6 MICRON FABRICATORS

LAMBDA=Ø.6 MICRONS

FOR 1.2 MICRON FABRICATORS

LAMBDA=Ø.5 MICRONS

FOR 1.Ø MICRON FABRICATORS

QUESTIONS TO FABRICATORS

MOSIS

MERGES CONTACT TO ACTIVE AND CONTACT TO POLY LAYERS TO GENERATE THE CONTACT MASK.

CAN APPLY BLOATS OR SHRINKS TO ALL LAYERS.

CAN ADJUST ACTIVE OVERLAP OF CONTACT INDEPENDENTLY OF BLOAT TO ACTIVE

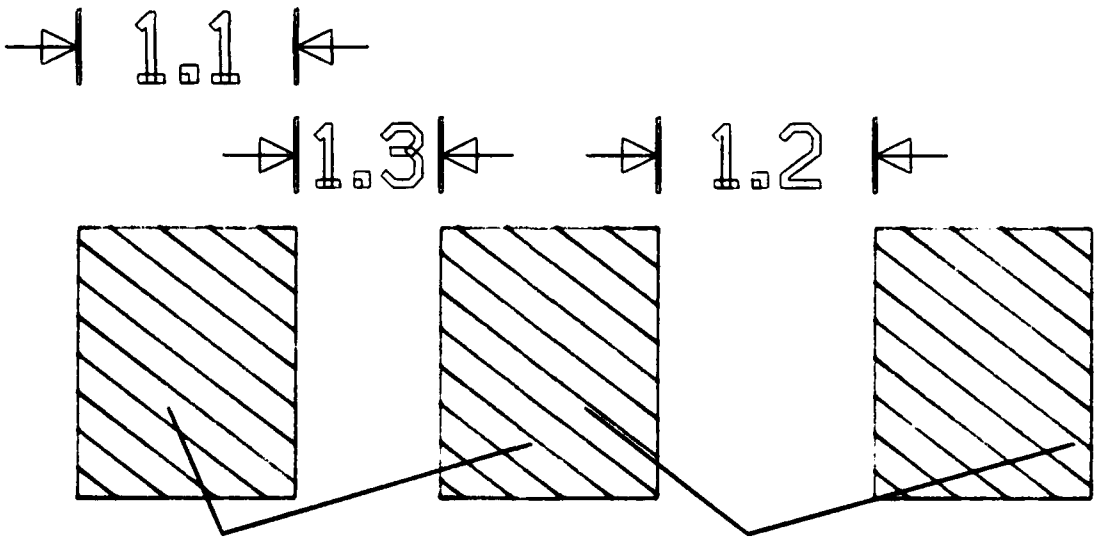
CAN ADJUST POLY OVERLAP OF CONTACT INDEPENDENTLY OF BLOAT TO POLY

FABRICATORS

WHAT VALUE OF LAMBDA CAN YOU SUPPORT? WHAT BLOATS OR SHRINKS DO YOU REQUIRE?

1. WELL
(NWELL.PWELL)

		LAMBDAS
1.1	WIDTH	10
1.2	SPACE DIFF. POT.	9
1.3	SPACE SAME POT.	0 OR 6

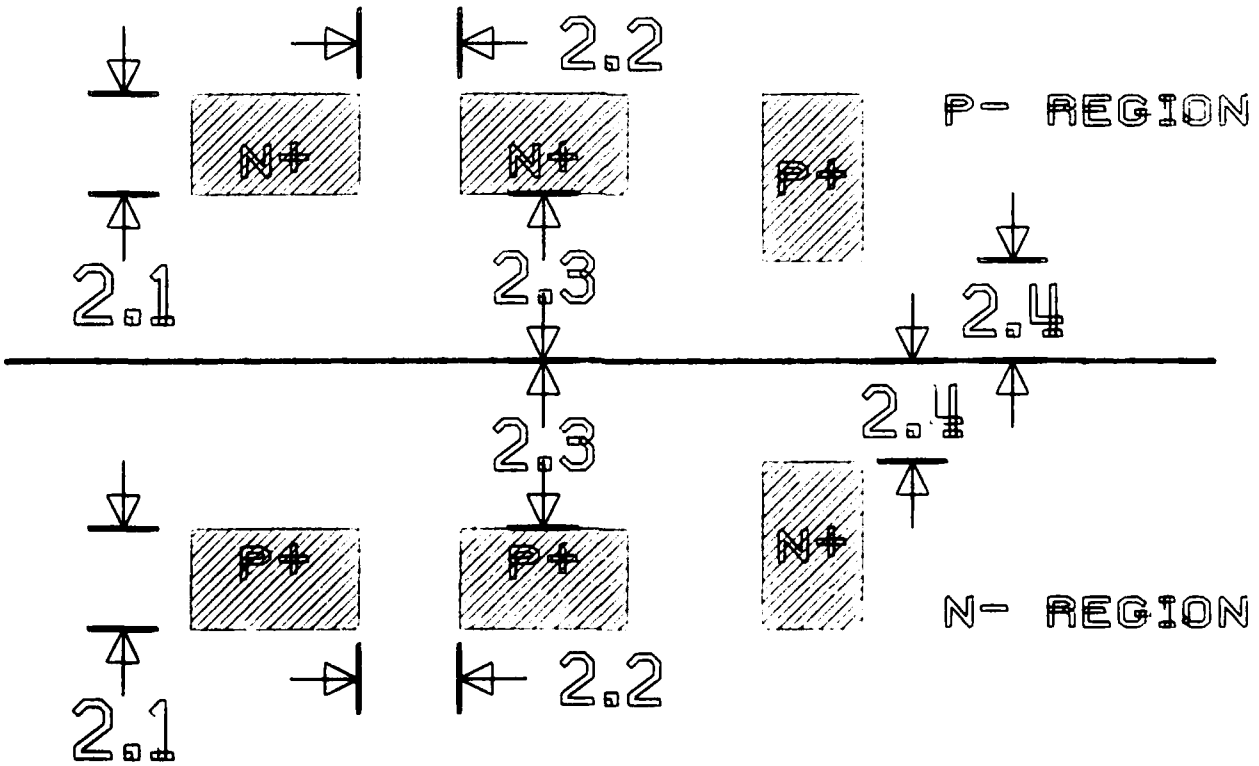


SAME POT. DIFF. POT.

NOTE: IF BOTH P AND N WELLS SUBMITTED, THEY MAY NOT OVERLAP BUT THEY MAY BE COINCIDENT.

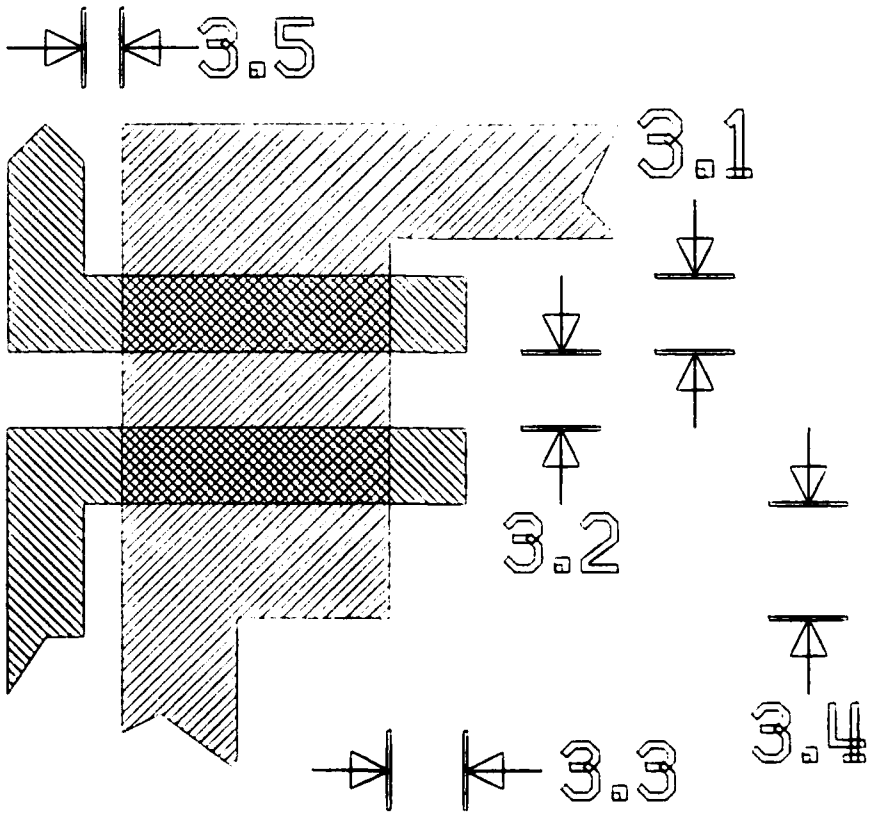
2. ACTIVE

		Lambdas
2.1	Width	3
2.2	Space	3
2.3	Source/Drain Active to Well Edge	5
2.4	Subs./Well Contact, Active to Well Edge	3



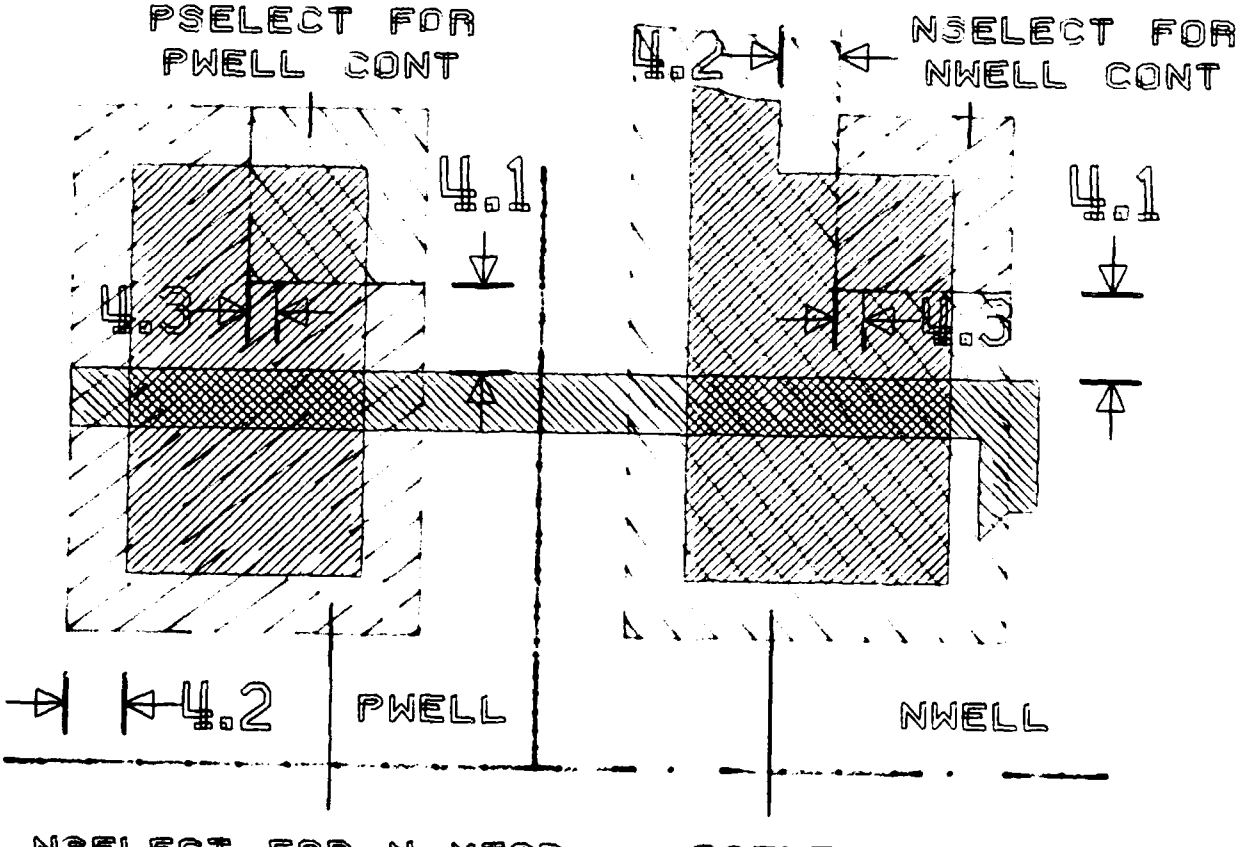
3. POLY

		Lambdas
3.1	Width	2
3.2	Space	2
3.3	Gate Overlap of Active	2
3.4	Active Overlap of Gate	3
3.5	Field Poly to Active	1



4. SELECT (PSELECT, NSELECT)

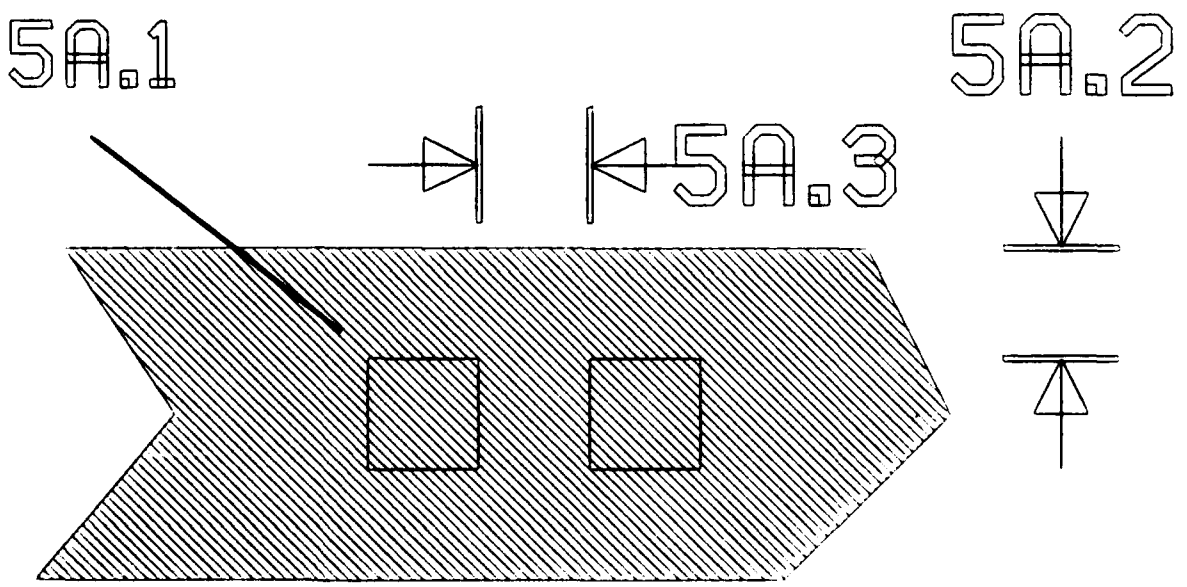
		LAMBDAS
4.1	SELECT SPACE (OVERLAP) TO (OF) CHANNEL TO ENSURE ADEQUATE SOURCE/DRAIN WIDTH	3
4.2	SELECT SPACE (OVERLAP) TO (OF) ACTIVE	2
4.3	SELECT SPACE (OVERLAP) TO (OF) CONTACT TO WELL OR SUBSTRATE	1
4.4	MIN WIDTH AND SPACE	2



NOTE: PSELECT AND NSELECT MAY BE COINCIDENT, BUT MUST NOT OVERLAP

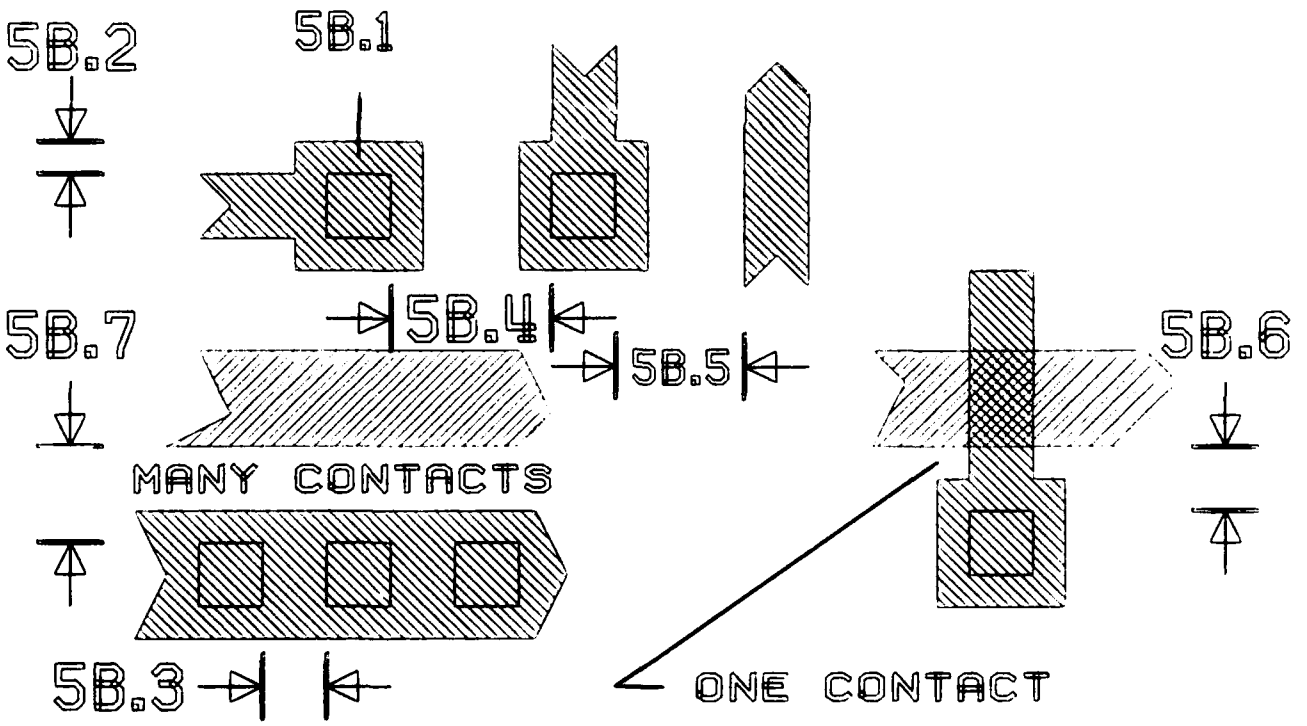
5A. SIMPLER CONTACT TO POLY

		LAMBDAS
5A.1	CONTACT SIZE EXACTLY	2x2
5A.2	POLY OVERLAP	2
5A.3	SPACING	2



5B. DENSER CONTACT TO POLY

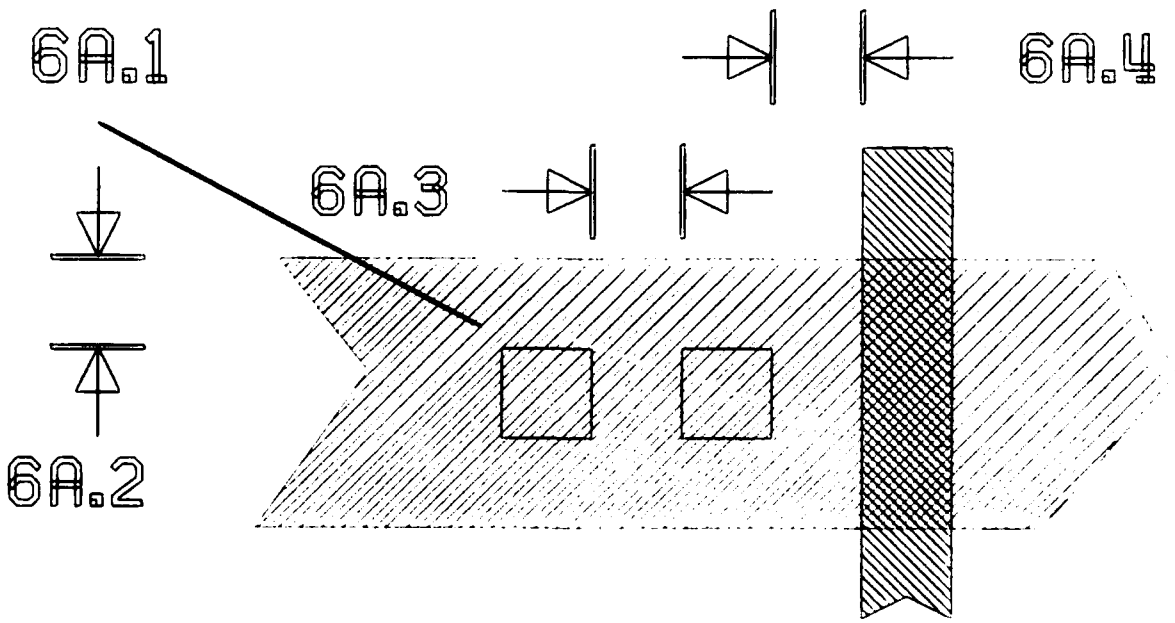
		LAMBDAS
5B.1	CONTACT SIZE, EXACTLY	2x2
5B.2	POLY OVERLAP OF CONTACT	1
5B.3	SPACING ON SAME POLY	2
5B.4	SPACING ON DIFF POLY	5
5B.5	SPACE TO OTHER POLY	4
5B.6	SPACE TO ACT. ONE CONTACT	2
5B.7	SPACE TO ACT. MANY CONTACTS	3



NOTE: YOUR ASSOCIATING CONTACTS WITH POLY OR ACTIVE ALLOWS MOSIS TO INDEPENDENTLY BLOAT THE LAYER AND THE LAYER OVERLAP OF THE CONTACT

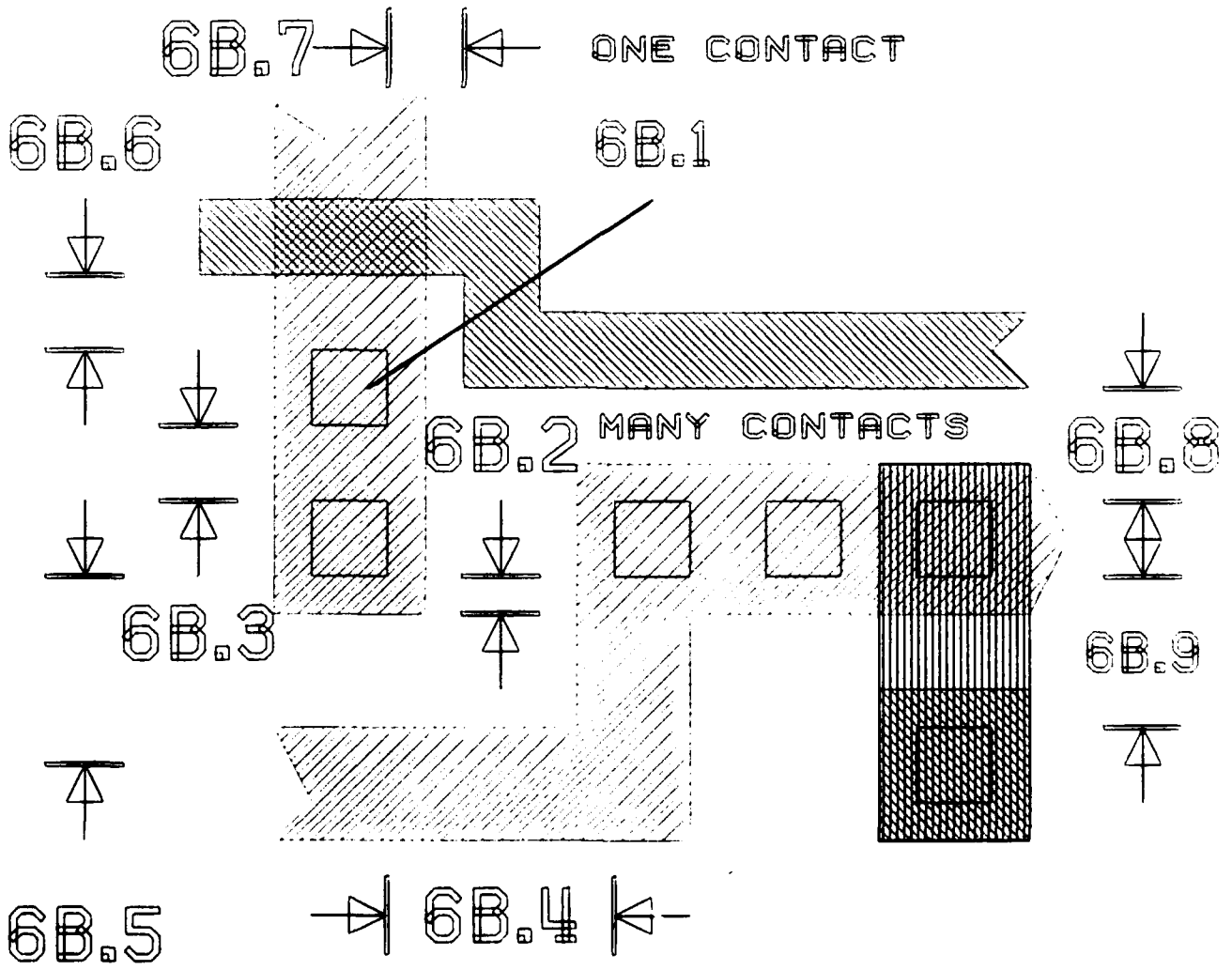
6A. SIMPLER CONTACT TO ACTIVE

		LAMBDAS
6A.1	CONTACT SIZE EXACTLY	2x2
6A.2	ACTIVE OVERLAP	2
6A.3	SPACING	2
6A.4	SPACE TO GATE	2



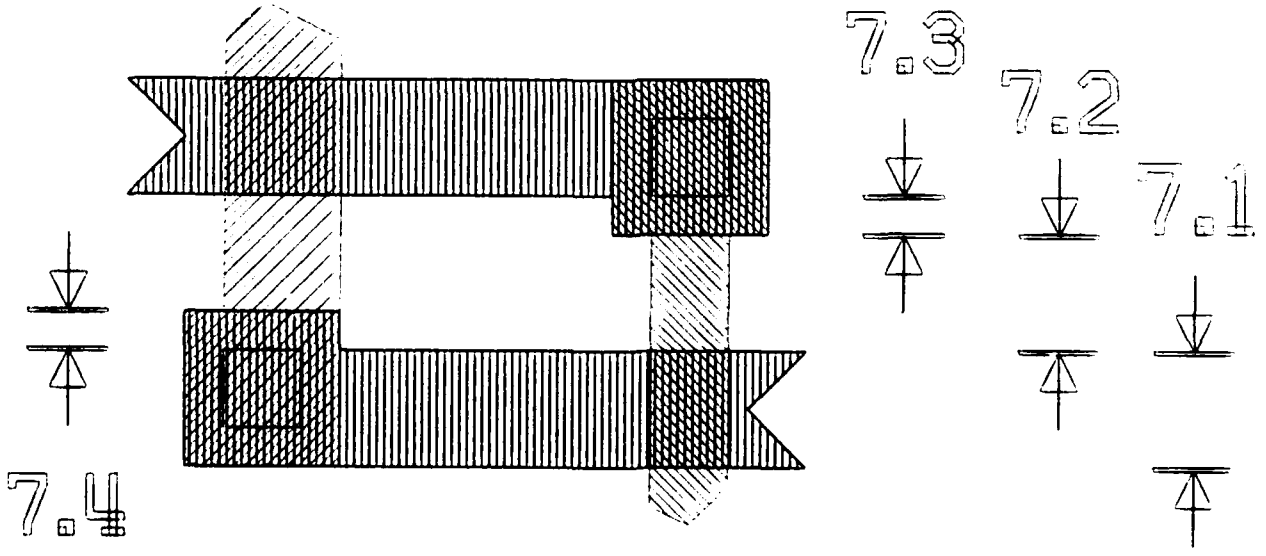
6B. DENSER CONTACT TO ACTIVE

		LAMBDAS
6B.1	CONTACT SIZE, EXACTLY	2X2
6B.2	ACTIVE OVERLAP	1
6B.3	SPACING ON SAME ACTIVE	2
6B.4	SPACING ON DIFF ACTIVE	6
6B.5	SPACE TO DIFF ACTIVE	5
6B.6	SPACE TO GATE	2
6B.7	SPACE TO FIELD POLY, ONE CONT.	2
6B.8	SPACE TO FIELD POLY, MANY CONT.	3
6B.9	SPACE TO CONTACT TO POLY	4



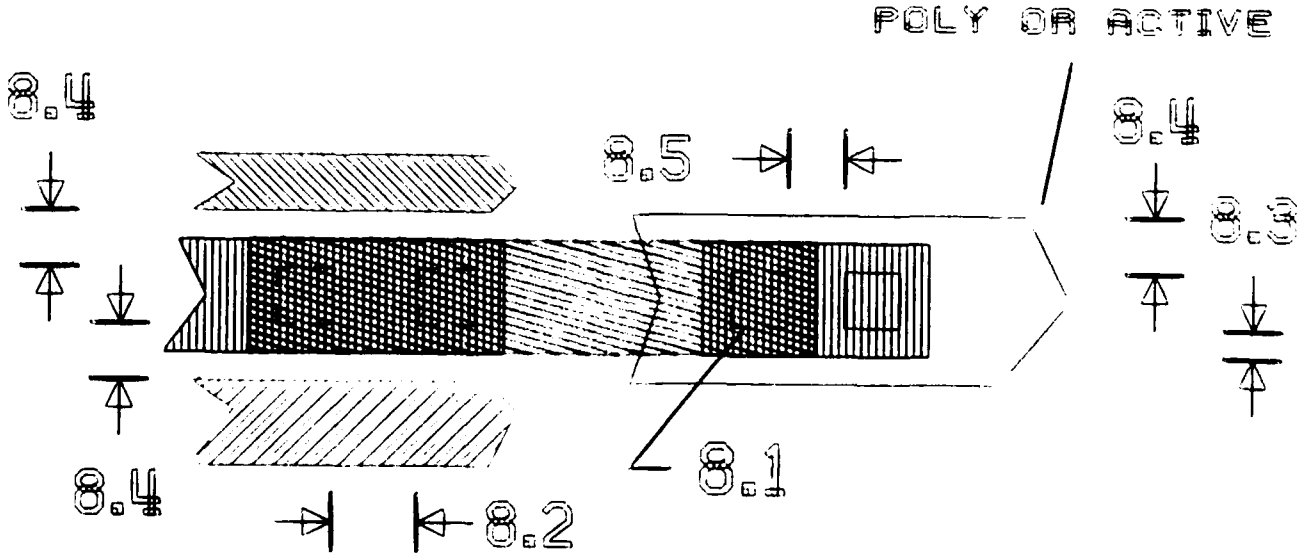
7. METAL1

		LAMBDAS
7.1	WIDTH	3
7.2	SPACE TO METAL1	3
7.3	OVERLAP OF CONTACT TO POLY	1
7.4	OVERLAP OF CONTACT TO ACTIVE	1



8. VIA

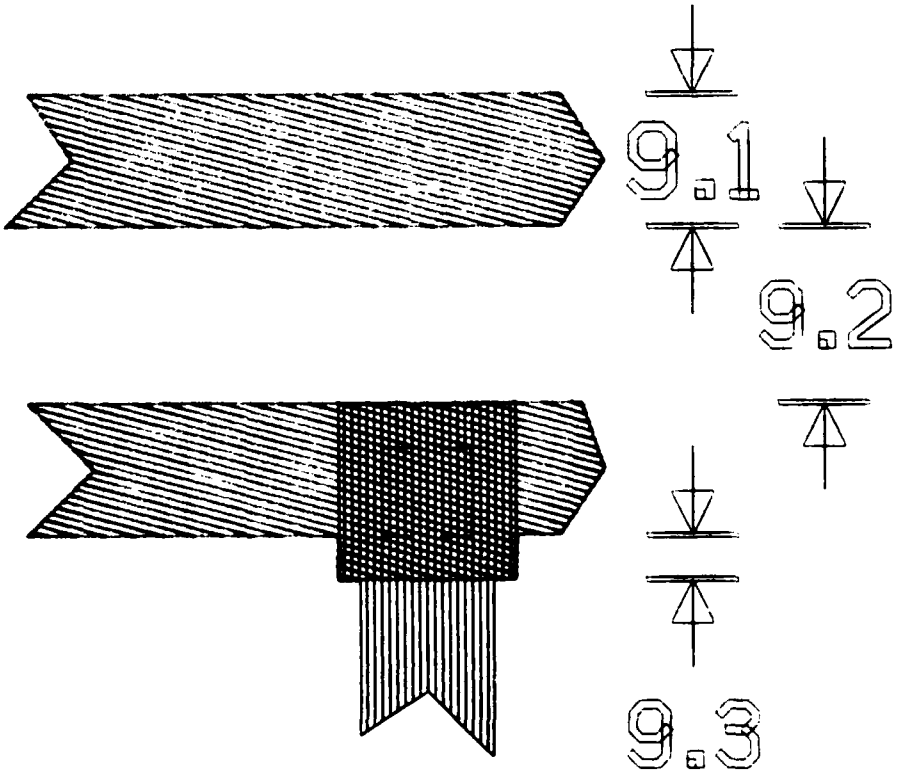
		LAMBDAS
8.1	SIZE, EXACTLY	2X2
8.2	SEPARATION TO VIA	3
8.3	OVERLAP BY METAL1	1
8.4	SPACE TO POLY OR ACTIVE EDGE	2
8.5	SPACE TO CONTACT	2



NOTE: OBJECTIVE IS VIA ON A FLAT SURFACE. VIA STACKED OVER CONTACT NOT ALLOWED.

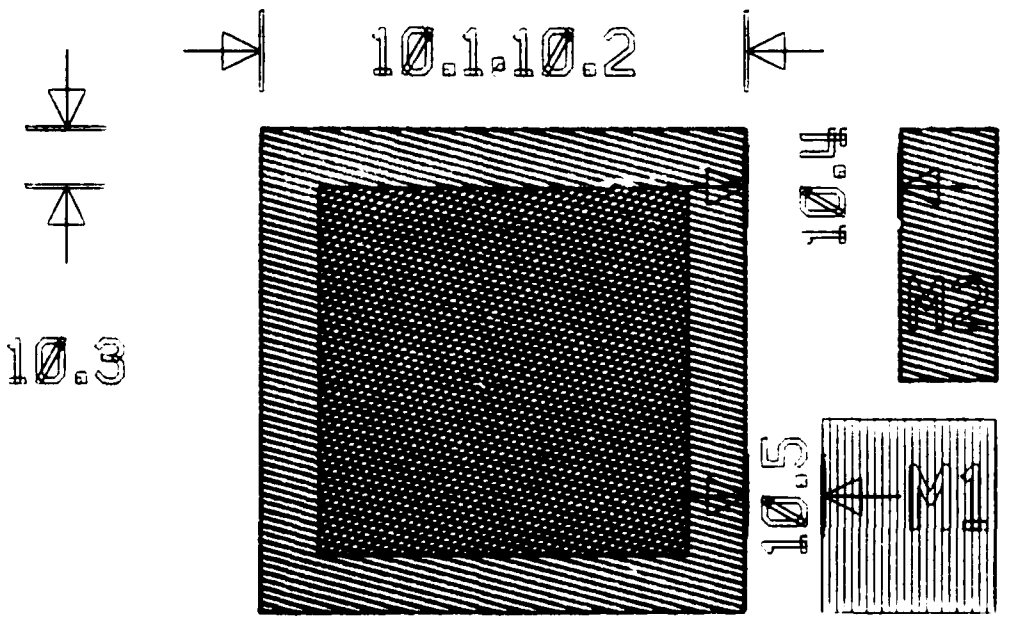
9. METAL2

		LAMBDAS
9.1	WIDTH	3
9.2	SPACE TO METAL2	4
9.3	OVERLAP OF VIA	1



10. OVERGLASS

		MICRONS
10.1	BONDING PAD	100×100
10.2	PROBE PAD	75×75
10.3	PAD OVERLAP OF GLASS	6
10.4	PAD SPACE TO UNRELATED METAL2	30
10.5	PAD SPACE TO UNRELATED METAL1, POLY OR ACTIVE	15



METAL2 REQUIRED UNDER OVERGLASS

MOSIS

CMOS ELECTRODE

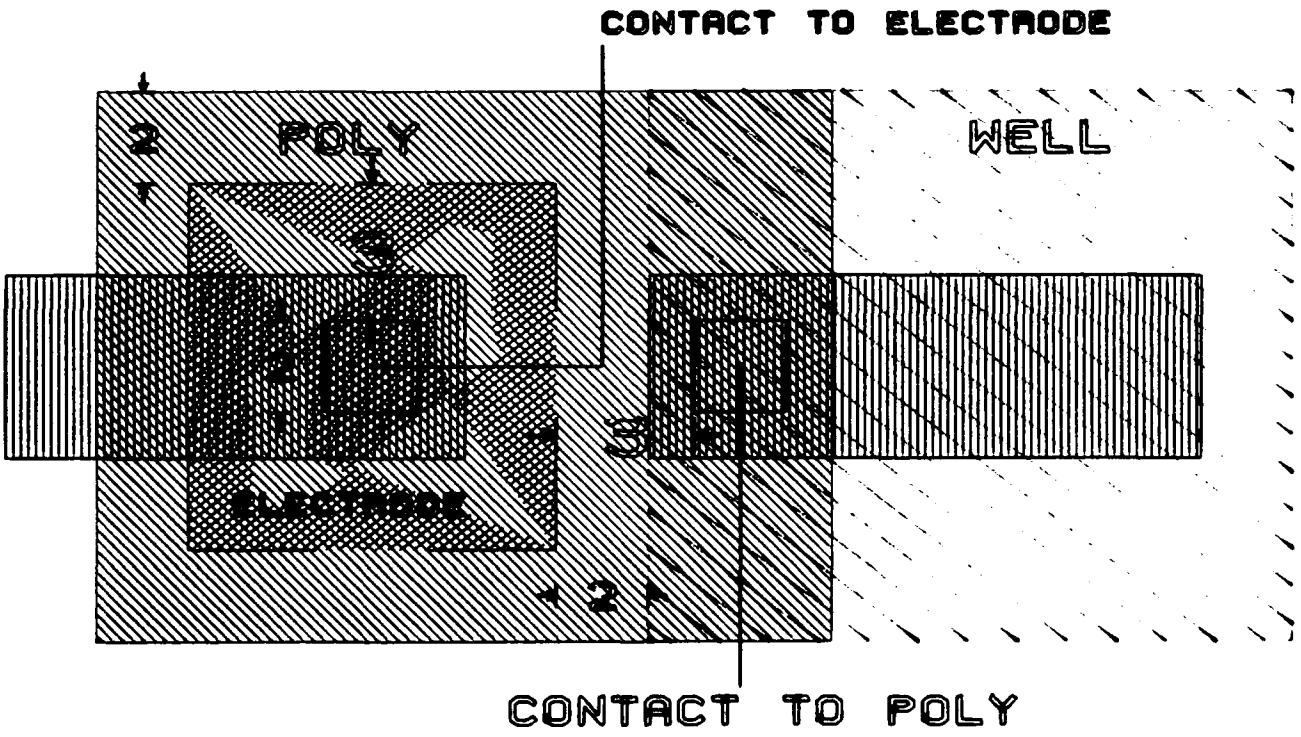
PRELIMINARY

DESIGN RULES

March 1989

11. ELECTRODE FOR CAPACITORS

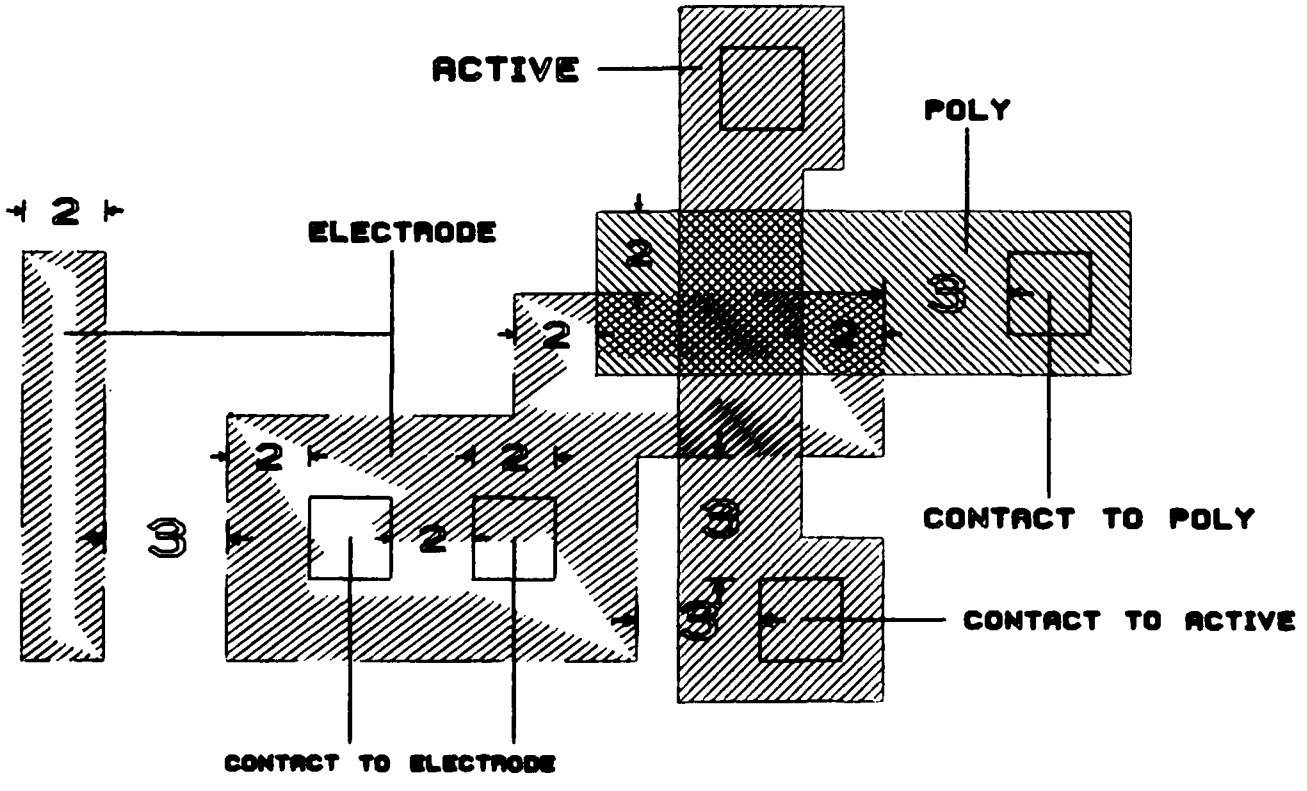
		LAMBDAS
11.1	WIDTH	3
11.2	SPACE	3
11.3	POLY OVERLAP OF	2
11.4	SPACE TO ACTIVE OR WELL EDGE	2
11.5	SPACE TO CONT TO POLY	3



CAPACITOR MUST BE ON FLAT SURFACE
SELECTS MAY NOT CROSS CAP PLATE

12. ELECTRODE FOR TRANSISTORS

		LAMBDAS
12.1	WIDTH	2
12.2	SPACE	3
12.3	GATE OVERLAP OF ACTIVE	2
12.4	SPACE TO ACTIVE	1
12.5	SPACE OR OVERLAP OF POLY	2
12.6	SPACE TO POLY OR ACTIVE CONTACT	3



13. ELECTRODE CONTACT

	LAMBDAS
13.1 Size	2
13.2 Space	2
13.3 Electrode Overlap of ON capacitor Plate	3
13.4 Electrode Overlap of NOT on capacitor Plate	2
13.5 Space to Poly or Active	3

See illustrations for ELECTRODE for CAPACITORS AND ELECTRODE for TRANSISTORS

ORBIT ELECTRICAL PARAMETERS

(2UM, 2 METAL, 2 POLY, P-WELL CMOS WITH 2ND POLY MAKING XTORS)

A. GENERAL SPECIFICATIONS

		MIN	TYP	MAX
A.1.1	Poly1 gate oxide thickness (angstroms)	370	400	430
A.1.2	Poly2 gate oxide thickness (angstroms)	470	500	530
A.2	Field oxide thickness (angstroms)	5500	6000	6500
A.3.1	Thickness of oxide between Metal1 and Poly1 (angstroms)	8000	8500	9000
A.3.2	Thickness of oxide between Metal1 and Poly2 (angstroms)	8000	8500	9000
A.4	Thickness of oxide between Metal2 and Metal1 (angstroms)	8500	10000	11000
A.5.1	Thickness of Poly1 (angstroms)	3500	4000	4500
A.5.2	Thickness of Poly2 (angstroms)	3500	4000	4500
A.6	Thickness of Metal1 (angstroms)	5500	6000	6500
A.7	Thickness of Metal2 (angstroms)	10500	11500	12500
A.8	Thickness of oxide between Poly1 and Poly2 over field (angstroms)	650	750	850
A.9	Thickness of oxide between Poly1 and Poly2 over active (angstroms)	650	750	850
A.10	Zero voltage N+/P- Junction capacitance (fF/micron^2)	0.15	0.18	0.25
A.11	Zero voltage N+/P- Junction peripheral cap. (fF/micron)	0.35	0.40	0.50
A.12	Zero voltage P+/N- Junction capacitance (fF/micron^2)	0.15	0.168	0.25
A.13	Zero voltage P+/N- Junction peripheral cap. (fF/micron)	0.30	0.40	0.50

B. TRANSISTOR SPECIFICATIONS

B.1	P Channel Poly1			
B.1.1	Threshold (volts)	-1.0	-0.8	-0.6
B.1.2	Gamma (volts ^.5)	0.4	0.5	0.6
B.1.3	K'=uCox/2 (uA/v^2)	6.0	7.0	8.0
B.1.4	Punchthrough for min. length channel (volts)	-25	-14	-10
B.1.5	Subthreshold slope (volts^-3/decade)			
B.1.6	Delta width = effective-mask (microns)	-1.0	-0.5	0
B.1.7	Delta length = effective-mask (microns)	-1.6	-1.2	-0.8
B.2	P Channel Poly2 (preliminary)			
B.2.1	Threshold (volts)	-1.5	-1.3	-1.1
B.2.2	Gamma (volts^.5)	0.5	0.6	0.7
B.2.3	K'=uCox/2 (uA/v^2)	5.0	6.0	7.0
B.2.4	Punchthrough for min. length channel (volts)	-25	-14	-10
B.2.5	Subthreshold slope (volts^-3/decade)			
B.2.6	Delta width = effective-mask (microns)	-1.0	-0.5	0
B.2.7	Delta length = effective-mask (microns)	-2.1	-1.7	-1.3
B.3	N Channel Poly1			
B.3.1	Threshold (volts)	0.6	0.8	1.0
B.3.2	Gamma (volts^.5)	0.8	1.0	1.2
B.3.3	K'=ucox/2 (uA/v^2)	21	23	25
B.3.4	Subthreshold slope (volts^-3/decade)			
B.3.5	Punchthrough for min. length channel (volts)	10	14	25
B.3.6	Delta width = effective-mask (microns)	-1.0	-0.5	0
B.3.7	Delta length = effective-mask (microns)	-1.75	-1.35	-0.95
B.4	N Channel Poly2 (preliminary)			
B.4.1	Threshold (volts)	0.3	0.5	0.7
B.4.2	Gamma (volts^.5)	0.8	1.1	1.4
B.4.3	K'=uCox/2 (uA/v^2)	17	18.5	20
B.4.4	Subthreshold slope (volts^-3/decade)			
B.4.5	Punchthrough for min. length channel (volts)	10	14	25
B.4.6	Delta width = effective-drawn (microns)	-1.0	-0.5	0
B.4.7	Delta length = effective-drawn (microns)	-2.25	-1.85	-1.45

		MIN	TYP	MAX
C.	SHEET RESISTANCES (OHMS PER SQUARE)			
C.1	P+ Active	60	75	100
C.2	N+ Active	10	20	30
C.3	P Well (with field implant)	1500	2000	2500
C.4.1	Poly1	15	25	40
C.4.2	Poly2	15	30	40
C.5	Metal1	.050	.070	.090
C.6	Metal2	.025	.050	.070
D.	CONTACT RESISTANCE (OHMS)			
D.1	Metal1 to P+ Active		35	75
D.2	Metal1 to N+ Active		45	75
D.3.1	Metal1 to Poly1		30	50
D.3.2	Metal1 to Poly2		30	50
D.4	Metal1 to Metal2 (single contact 2 by 2um)		0.4	0.7
E.	FIELD INVERSION AND BREAKDOWN VOLTAGES (VOLTS)			
E.1.1	N Channel Poly1 field inversion	10	15	20
E.1.2	N Channel Poly2 field inversion	10	14	20
E.2	N Channel Metal1 field inversion	12	15	20
E.3	N Channel Metal2 field inversion	12		
E.4.1	Channel Poly1 field inversion	10	12	20
E.4.2	P Channel Poly2 field inversion	10	11	20
E.5	P Channel Metal1 field inversion	12		
E.6	P Channel Metal2 field inversion	12		
E.7	N+ to well breakdown	15	18	
E.8	P+ to substrate breakdown	|15|	|20|	

INTERLAYER CAPACITANCES

(PLATE: 10^-5 PFS MICRON ^-2 FRINGE: 10^-5 PFS MICRON ^2)

	Capacitance		Equiv. Thickness	
	MIN	MAX	MIN	MAX
GATE OXIDE PLATE POLY1	80	100	350 Ang	450 Ang
GATE OXIDE PLATE POLY2	59	70	450 Ang	550 Ang
FIELD POLY1 TO SUBS FRINGE				
FIELD POLY2 TO SUBS FRINGE				
POLY1 TO POLY2 OVER ACTIVE	40	50	700 Ang	800 Ang
POLY1 TO POLY2 OVER FIELD	40	50	700 Ang	800 Ang
METAL1 TO ACTIVE PLATE	3.7	3.7	0.8 um	1.0 um
METAL1 TO ACTIVE FRINGE				
METAL1 TO SUBS PLATE	2.0	2.2	1.35 um	1.5 um
METAL1 TO POLY PLATE	3.3	3.7	0.8 um	1.0 um
METAL1 TO POLY FRINGE				
METAL2 TO ACTIVE PLATE	1.5	1.7	1.8 um	2.0 um
METAL2 TO ACTIVE FRINGE				
METAL2 TO SUBS PLATE	1.14	1.28	2.35 um	2.65 um
METAL2 TO SUBS FRINGE				
METAL2 TO POLY PLATE	1.45	1.7	1.8 um	2.1 um
METAL2 TO POLY FRINGE				
METAL2 TO METAL1 PLATE	2.9	3.4	0.9 um	1.05 um
METAL2 TO METAL1 FRINGE				

B. TRANSISTOR SPECIFICATIONS

B.1 P Channel Poly1

B.1.1	Threshold (volts)	-1.0	-0.8	-0.6
B.1.2	Gamma (volts ^.5)	0.4	0.5	0.6
B.1.3	K'=uCox/2 (uA/v^2)	6.0	7.0	8.0
B.1.4	Punchthrough for min. length channel (volts)	-25	-14	-10
B.1.5	Subthreshold slope (volts^-3/decade)			
B.1.6	Delta width = effective-mask (microns)	-1.0	-0.5	0
B.1.7	Delta length = effective-mask (microns)	-1.6	-1.2	-0.8

B.2 P Channel Poly2 (preliminary)

B.2.1	Threshold (volts)	-1.5	-1.3	-1.1
B.2.2	Gamma (volts^.5)	0.5	0.6	0.7
B.2.3	K'=uCox/2 (uA/v^2)	5.0	6.0	7.0
B.2.4	Punchthrough for min. length channel (volts)	-25	-14	-10
B.2.5	Subthreshold slope (volts^-3/decade)			
B.2.6	Delta width = effective-mask (microns)	-1.0	-0.5	0
B.2.7	Delta length = effective-mask (microns)	-2.1	-1.7	-1.3

B.3 N Channel Poly1

B.3.1	Threshold (volts)	0.6	0.8	1.0
B.3.2	Gamma (volts^.5)	0.8	1.0	1.2
B.3.3	K'=ucox/2 (uA/v^2)	21	23	25
B.3.4	Subthreshold slope (volts^-3/decade)			
B.3.5	Punchthrough for min. length channel (volts)	10	14	25
B.3.6	Delta width = effective-mask (microns)	-1.0	-0.5	0
B.3.7	Delta length = effective-mask (microns)	-1.75	-1.35	-0.95

B.4 N Channel Poly2 (preliminary)

B.4.1	Threshold (volts)	0.3	0.5	0.7
B.4.2	Gamma (volts^.5)	0.8	1.1	1.4
B.4.3	K'=uCox/2 (uA/v^2)	17	18.5	20
B.4.4	Subthreshold slope (volts^-3/decade)			
B.4.5	Punchthrough for min. length channel (volts)	10	14	25
B.4.6	Delta width = effective-drawn (microns)	-1.0	-0.5	0
B.4.7	Delta length = effective-drawn (microns)	-2.25	-1.85	-1.45

		MIN	TYP	MAX
C.	SHEET RESISTANCES (OHMS PER SQUARE)			
C.1	P+ Active	60	75	100
C.2	N+ Active	10	20	30
C.3	P Well (with field implant)	1500	2000	2500
C.4.1	Poly1	15	25	40
C.4.2	Poly2	15	30	40
C.5	Metal1	.050	.070	.090
C.6	Metal2	.025	.050	.070
D.	CONTACT RESISTANCE (OHMS)			
D.1	Metal1 to P+ Active		35	75
D.2	Metal1 to N+ Active		45	75
D.3.1	Metal1 to Poly1		30	50
D.3.2	Metal1 to Poly2		30	50
D.4	Metal1 to Metal2 (single contact 2 by 2um)		0.4	0.7
E.	FIELD INVERSION AND BREAKDOWN VOLTAGES (VOLTS)			
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E.2	N Channel Metal1 field inversion	12	15	20
E.3	N Channel Metal2 field inversion	12		
E.4.1	Channel Poly1 field inversion	10	12	20
E.4.2	P Channel Poly2 field inversion	10	11	20
E.5	P Channel Metal1 field inversion	12		
E.6	P Channel Metal2 field inversion	12		
E.7	N+ to well breakdown	15	18	
E.8	P+ to substrate breakdown	|15|	|20|	

INTERLAYER CAPACITANCES

(PLATE: 10^-5 PFS MICRON ^-2 FRINGE: 10^-5 PFS MICRON ^2)

	Capacitance		Equiv. Thickness	
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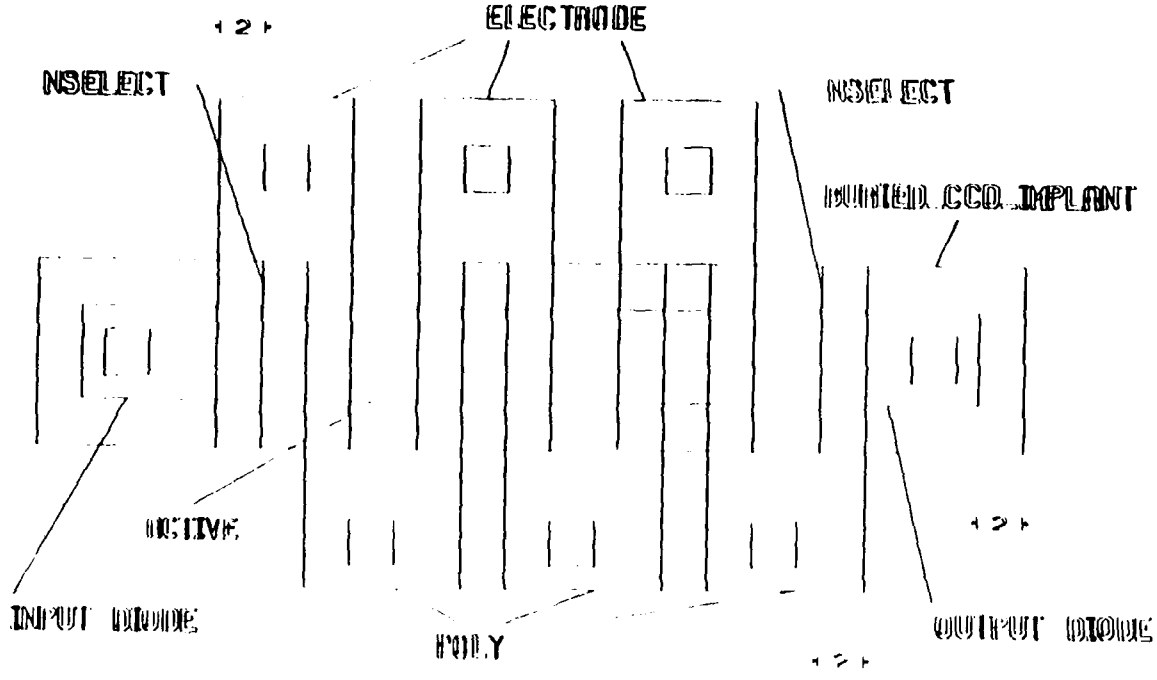
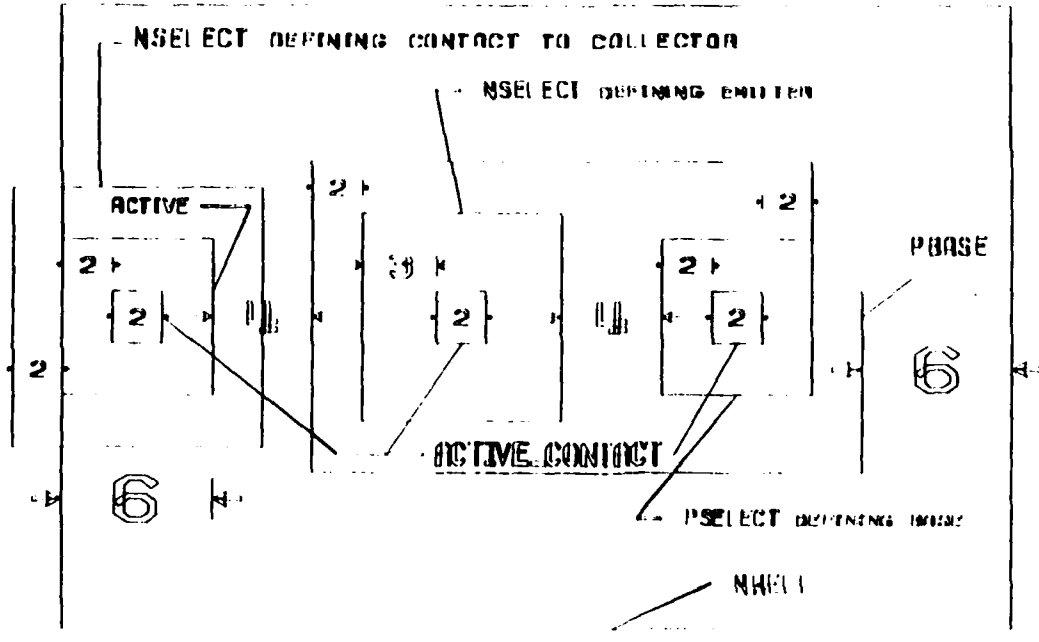
FIELD POLY1 TO SUBS FRINGE				
FIELD POLY2 TO SUBS FRINGE				
POLY1 TO POLY2 OVER ACTIVE	40	50	700 Ang	800 Ang
POLY1 TO POLY2 OVER FIELD	40	50	700 Ang	800 Ang
METAL1 TO ACTIVE PLATE	3.7	3.7	0.8 um	1.0 um
METAL1 TO ACTIVE FRINGE				
METAL1 TO SUBS PLATE	2.0	2.2	1.35 um	1.5 um
METAL1 TO POLY PLATE	3.3	3.7	0.8 um	1.0 um
METAL1 TO POLY FRINGE				
METAL2 TO ACTIVE PLATE	1.5	1.7	1.8 um	2.0 um
METAL2 TO ACTIVE FRINGE				
METAL2 TO SUBS PLATE	1.14	1.28	2.35 um	2.65 um
METAL2 TO SUBS FRINGE				
METAL2 TO POLY PLATE	1.45	1.7	1.8 um	2.1 um
METAL2 TO POLY FRINGE				
METAL2 TO METAL1 PLATE	2.9	3.4	0.9 um	1.05 um
METAL2 TO METAL1 FRINGE				

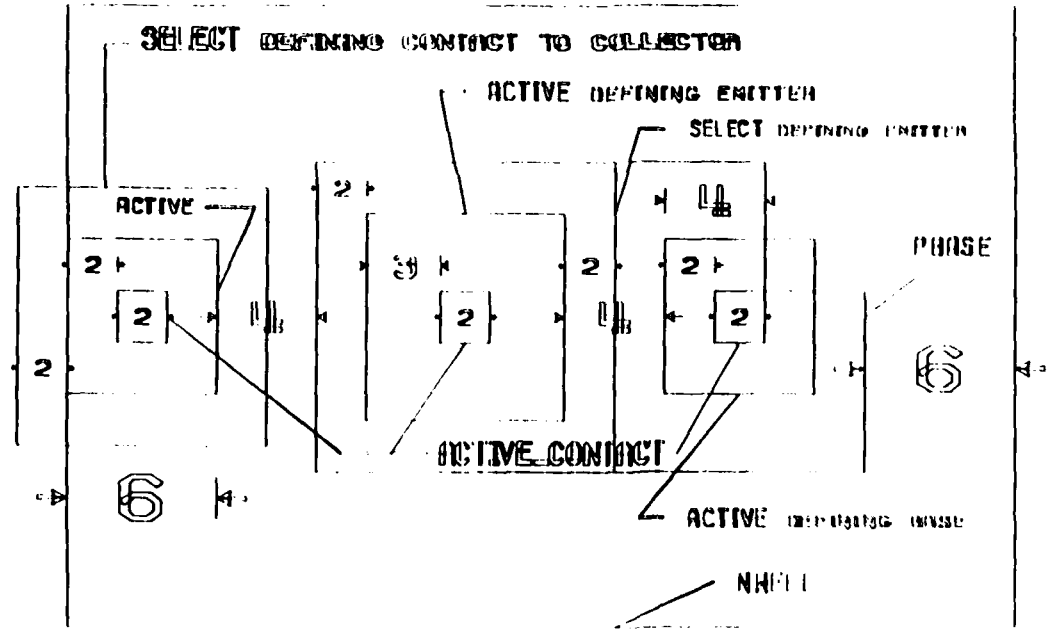
BURIED CHANNEL CCD RULES



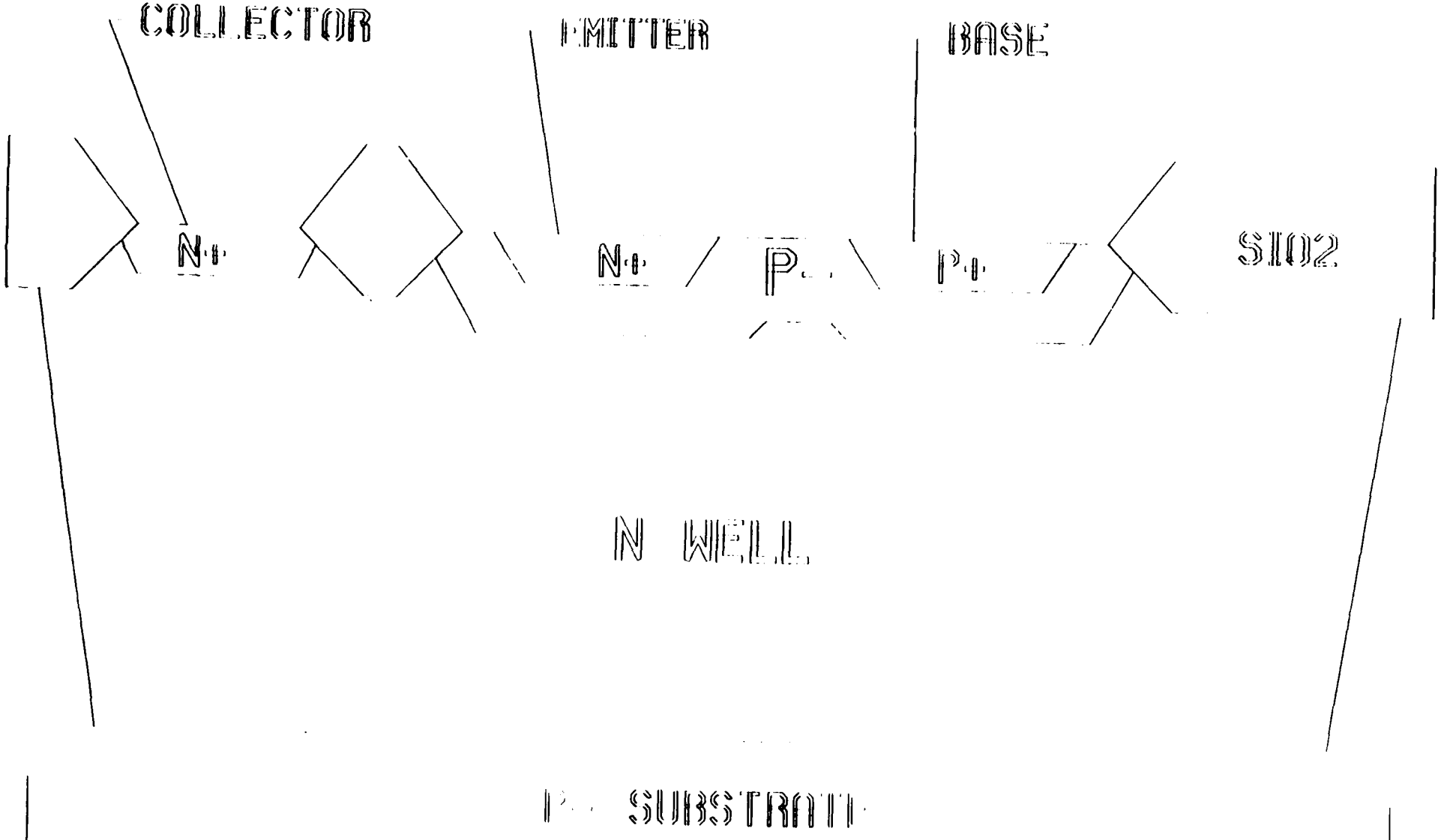
2 MICRON NPN TRANSISTOR RULES BASED ON SCEN LAYERS



2 MICRON NPN TRANSISTOR RULES BASED ON SCGH LAYERS



NPN TRANSISTOR CROSS SECTION



MOSIS' 2.0 Micron TinyChip

Version 1.0

This floppy includes the layout of 2.0 micron TinyChip pad frame cells, MOSIS' scalable design rules (Revision 6), electrical parameters from current MOSIS 2.0 micron vendors, CIF and documentation files for N and P well pad frame cells and sample SPICE (Level 2) and BSIM transistor models.

TinyChip 2.0 Micron Project Specifications

The 2.0 micron TinyChip project size is 2220 x 2250 microns. Projects must be submitted as 'TINY-technology' name (e.g., TINY-SCN) on your Project Submission Form which you mail with your magnetic tape, or if you are sending your project via netmail, in your messages to MOSIS.

Use of a MOSIS Standard Frame (a frame with predesigned pads) is no longer required as long as the number of pads is 40 or less. The standard frame requirement was changed to accomodate the use of the CMOSN standard cell library pads (for TINY-NSCE projects); because of the width of these pads, 40 of them won't fit into a 2um TinyChip. Make sure to specify EITHER a Standard Frame OR the SIZE and PAD COUNT on your Project Submission Form.

If you do not use a standard frame, MOSIS will do a bondability check when the project is submitted to (1) confirm that the number of pads is 40 or less, and (2) make sure a bonding diagram can be generated automatically by MOSIS. Projects will be packaged as follows:

- 1 - 28 pads: 28-pin DIP
- 29 - 40 pads: 40-pin DIP
- 0 pads: Parts will not be packaged
- 40+ pads: MOSIS will ask designer to resubmit project with 40 pads or less.

The MOSIS TinyChip Standard Frame has pads available in .CIF file format (SCN2U_PADS and SCP2U_PADS).

A "Stuffed" version ("Stufdpad.cif" on the floppy) of the Standard Frame has been developed for each well. The 40 pins include 3 Vdd (#5, #15, and #30), 3 GND pins (#10, #25, and #35) and 34 I/O pads. Available design area inside the pad circuitry is 1800 x 1830 microns. This "Stuffed" frame is an example of how pads may be placed (although different combinations are possible).

PLEASE NOTE: Vendor specifications and SPICE and BSIM decks in this packet are subject to change.

Contents of the Diskette

Files on this floppy are compressed. You will need at least 1 Megabyte of space to uncompress the files. Type the file called "Contents" for a list of files and instructions on how to uncompress them.

Chip Assembly

You will receive bonded and packaged parts unless you specifically request 'UNPACKAGED PARTS' in your Project Submission Form. To request unpackaged parts when you are submitting your project via Email, use the parameter "PADS:0". The cost is the same whether your parts are packaged or unpackaged.

Substrate

There is no substrate connection to the GND pin (N well) or VDD pin (P well). It is your responsibility to place both well and substrate contacts in your design.

Contacts

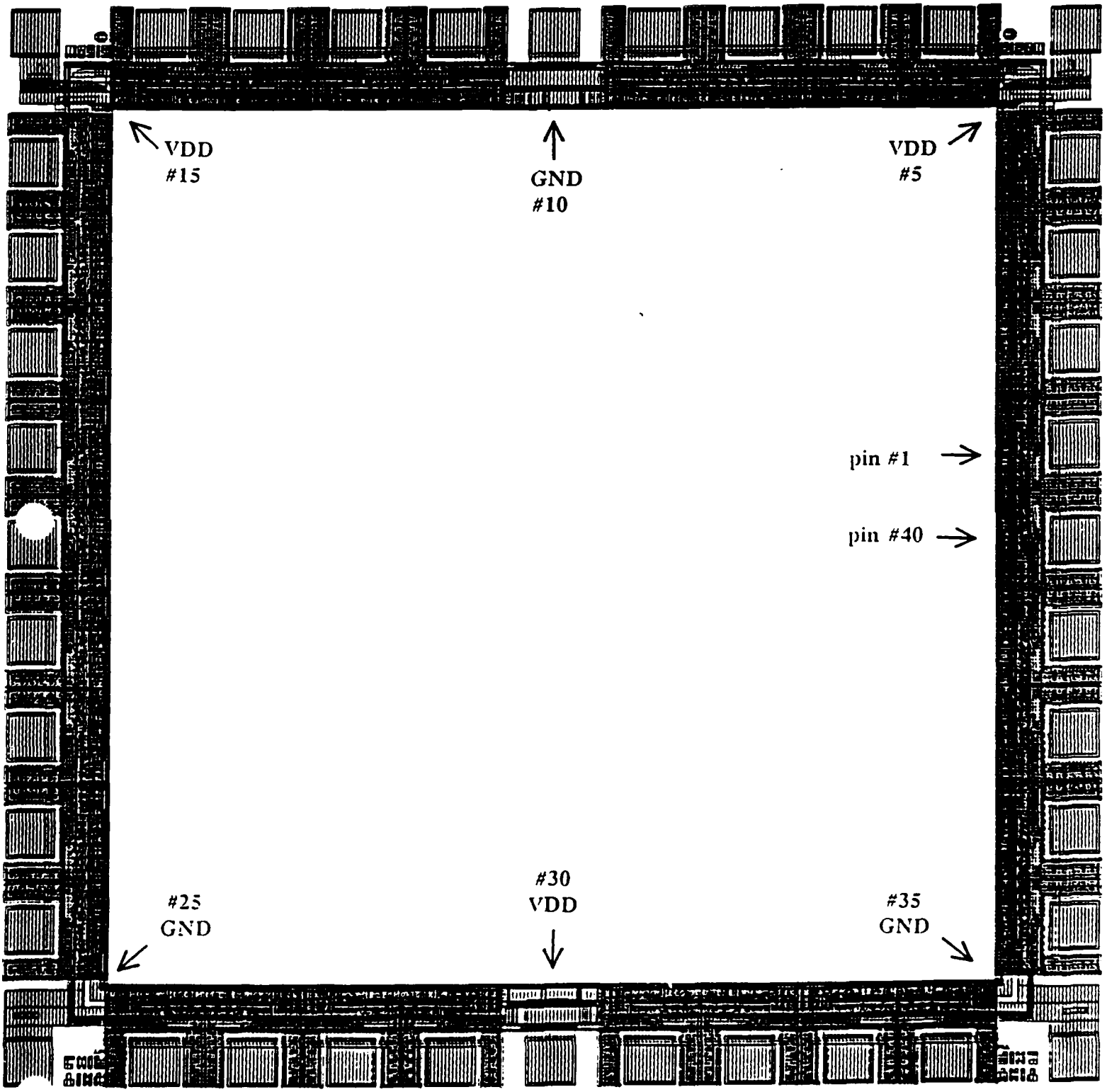
If you have any questions regarding this material, please contact Sam Delatorre at (213) 822-1511.

102689ct

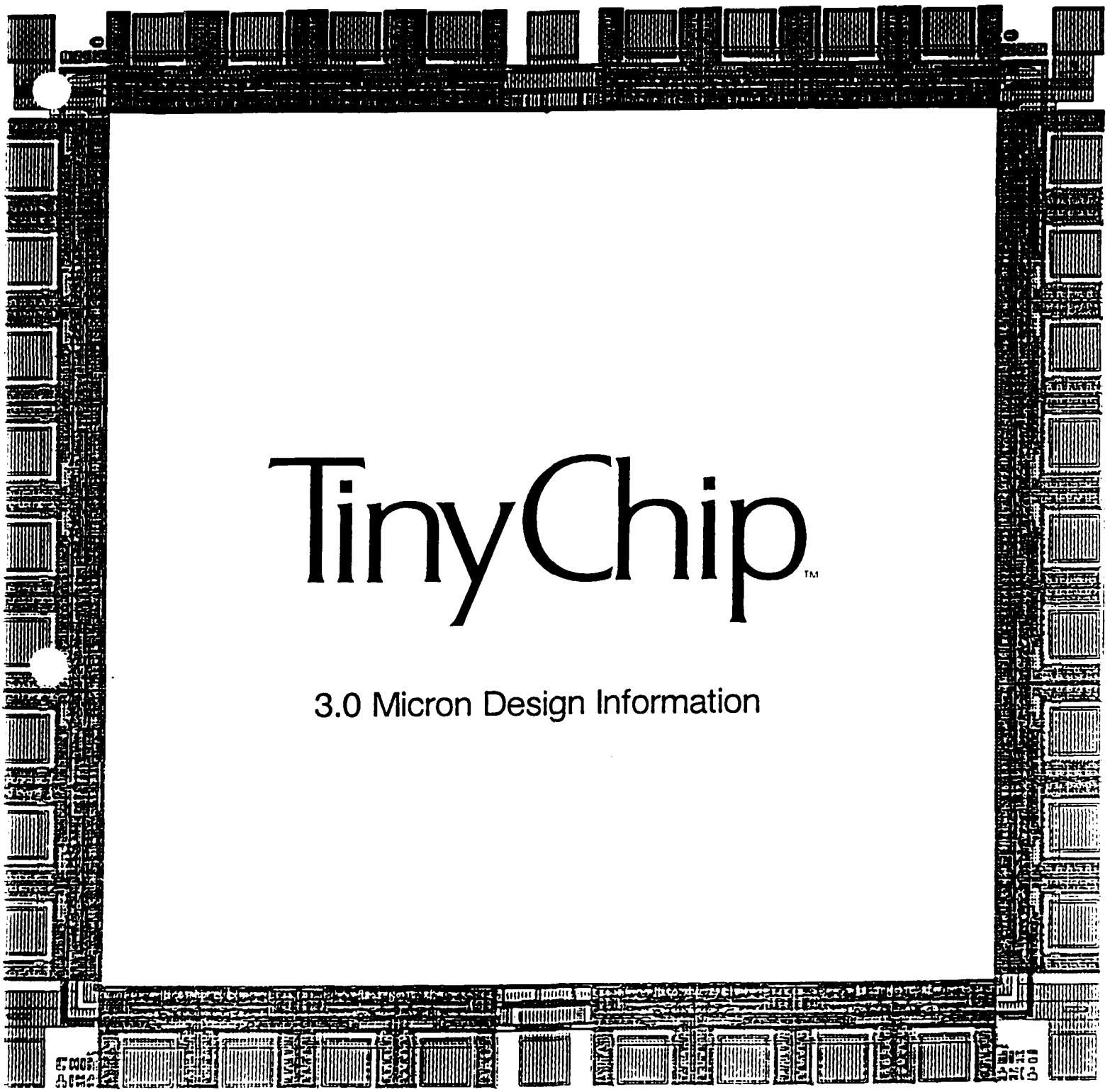
master

TinyChip 2.0um "Stuffed" Pad Frame

40PC22x22



Available Design Area: 1800 x 1830 microns



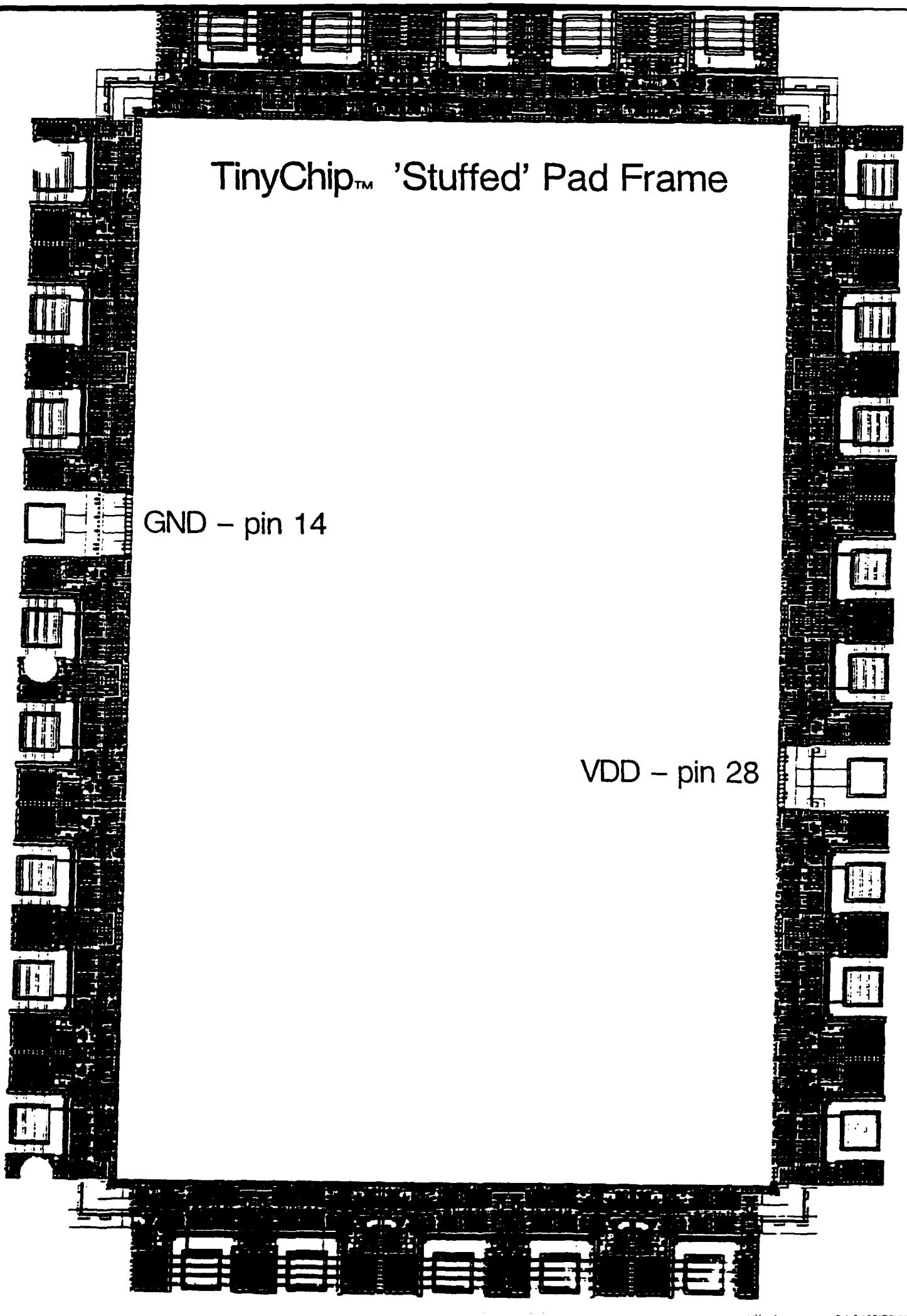
TinyChip™

3.0 Micron Design Information

USC/Information Sciences Institute, 4676 Admiralty Way, Marina del Rey, CA 90292-6695. Telephone: (213) 822-1511.

MOSIS.

TinyChip™ 'Stuffed' Pad Frame



TinyChip$_{TM}$ Design Information

Introduction

This packet includes the layout of TinyChip pad frame cells, MOSIS' recent versions of scalable (Revision 6) and nonscalable (Revision 2) design rules as well as electrical parameters supplied by current MOSIS vendors. The diskette also includes CIF and documentation files for the pad frame cells and sample SPICE (Level 2) transistor models which have been derived from MOSIS runs over the last year.

TinyChip projects use 3 micron CMOS P well (scalable and nonscalable) processes and must use the TinyChip Standard Pad Frame. See the sections below for more information on TinyChip specifications.

Contents of the TinyChip Projects' Diskette

1. This file:
    a. Read.Me
2. CIF and documentation files for the TinyChip Pad Frame pad locations.
    a. 28PC2334.CIF (CIF for the TinyChip Frame.)
    b. 28PC2334.LIS (pad locations for the TinyChip Frame.)
3. TinyChip CIF file sets, documentation and a set of IO pads positioned in a Standard Frame) (for SCP technology only, i.e., TINY-SCP).
    a. TINYPADS.DOC
    b. CORNER.CIF
    c. PADBLNK.CIF
    d. PADGND.CIF
    e. PADIN.CIF
    f. PADIO.CIF
    g. PADOUT.CIF
    h. PADVDD.CIF
    i. SPACER.CIF
    j. STUFFED.CIF (Complete CIF layout for the IO pads in a Standard Frame.)

TinyChip$_{TM}$ Pads Set

SCMOS (P Well) 3 Micron

Introduction

This 3 micron SCMOS (P-well) TinyChip pads set was designed with the MOSIS scalable CMOS design rules at a lambda of 1.5 microns. All pads are laid out on a lambda grid and are designed to be used with the 28PC23x34 Standard Frame. When submitting a project to MOSIS using this pad set, you must specify the technology as 'TINY-SCP'.

Contents of Pads Set

- TINY_SCP3U_PADS.CIF contains 8 cells (6 pads plus 2 auxiliary cells).
  - CORNER.CIF
  - PADBLANK.CIF
  - PADGND.CIF
  - PADIN.CIF
  - PADIO.CIF
  - PADOUT.CIF
  - PADVDD.CIF
  - SPACER.CIF
- 28PC23X34_STUFFED.CIF contains a complete pad ring layout, sized 2300x3400um.

Description of Pads

Size

There are six pads in this pad set; the first is the I/O pad. This pad has a non-well maximum bounding box of 218x192 lambda; the non-well bounding box is the bounding box minus the well and the select layer measurements. Modified versions of this pad exist for Input and Output; they are Padin and Padout (see Connections section below). There is also a blank pad which has no I/O connections. The other two pads are the Vdd and the Ground pad. Both of them have a non-well width of lambda 116. These pads are to be used for the MOSIS 28PC23x34 Standard Frame. This frame has 28 pins with 5 pins on each of the top and bottom edges, and 9 pins on each of the right and left edges. Two auxiliary cells, CORNER and SPACER, complete the pad frame.

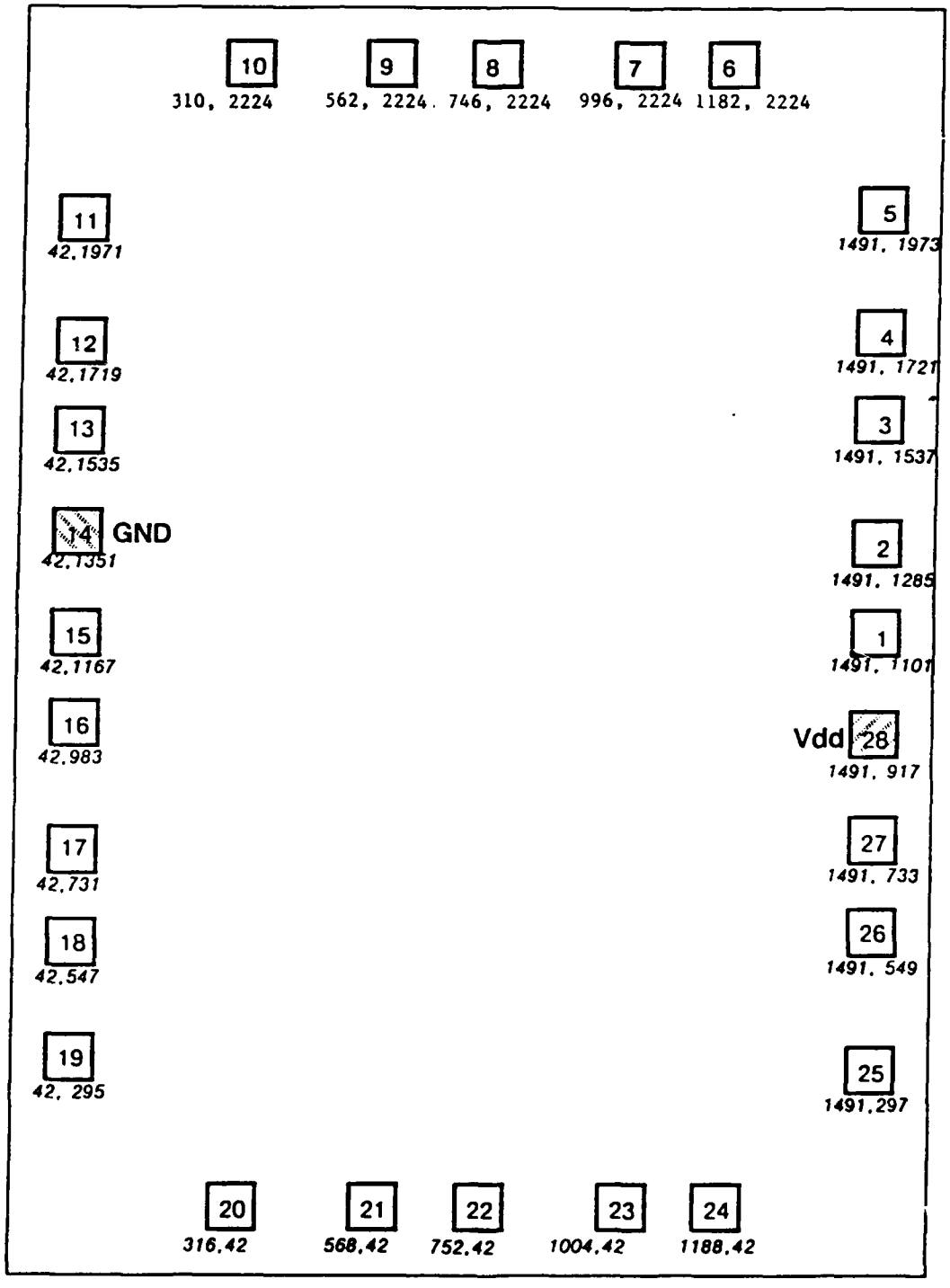
A frame with all 28 IO pads in preset locations, the 'Stuffed' Frame is available from MOSIS and is in the file 28PC23X34_STUFFED.CIF. Pin #14 is Ground and pin #28 is Vdd; the other 26 pins are I/O. The total frame size (non-well MBB) is 1533 x 2266 lambda (or 2299.5 x 3399 microns).

Protection

The input protection on the I/O pad consists of a P+ to substrate diode and a N+ to well diode, which are both also used as output drivers. These two diodes provide voltage clipping ability. When input voltage is higher than Vdd or lower than Ground, these two diodes will turn on respectively to give the proper protection.

3.0um TinyChip Standard Frame Pad Locations

Pad Center Positions (in Lambda)



Size: 2300 x 3400 microns (1533 x 2266 Lambda)

WAFER ACCEPTANCE SPECIFICATIONS FOR

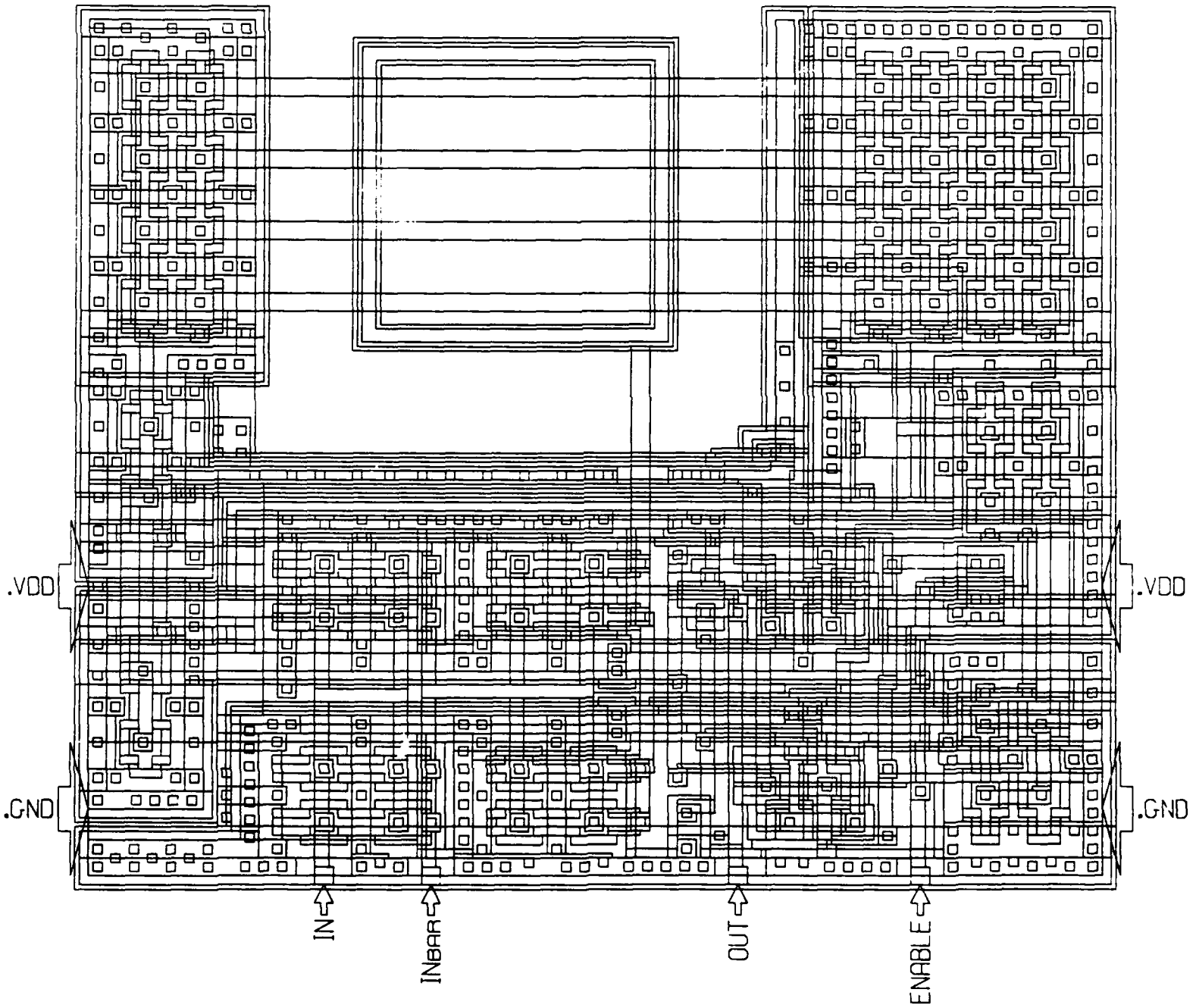
HP CMOSH 2.5 micron CMOS Bulk Wafers

Wafer acceptance is based on 3 measurements of the 8039 parametric test insert on every wafer. The wafer summary will be sent to MOSIS with the wafers. This document includes one section for the wafer acceptance specifications and another section for general process specifications. The general process specifications are included to provide simulation information for MOSIS customers. NID does not base wafer acceptance on the general process specifications.

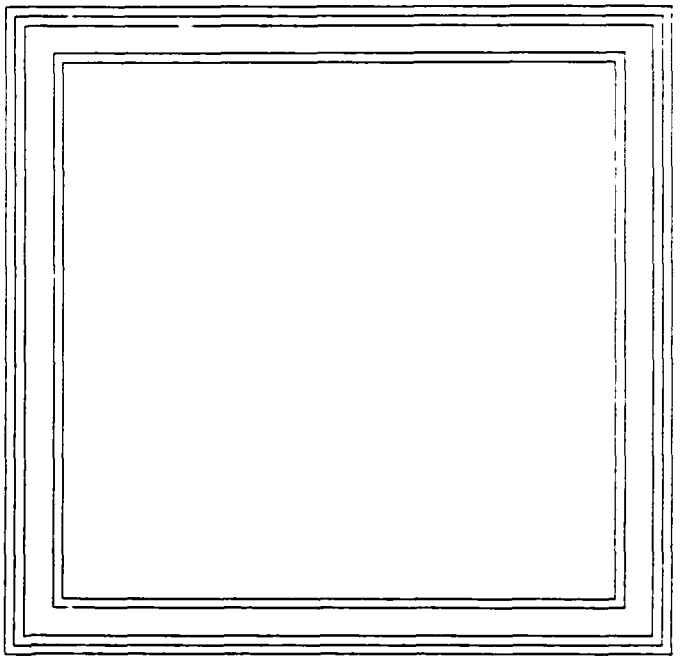
WAFER ACCEPTANCE SPECIFICATIONS

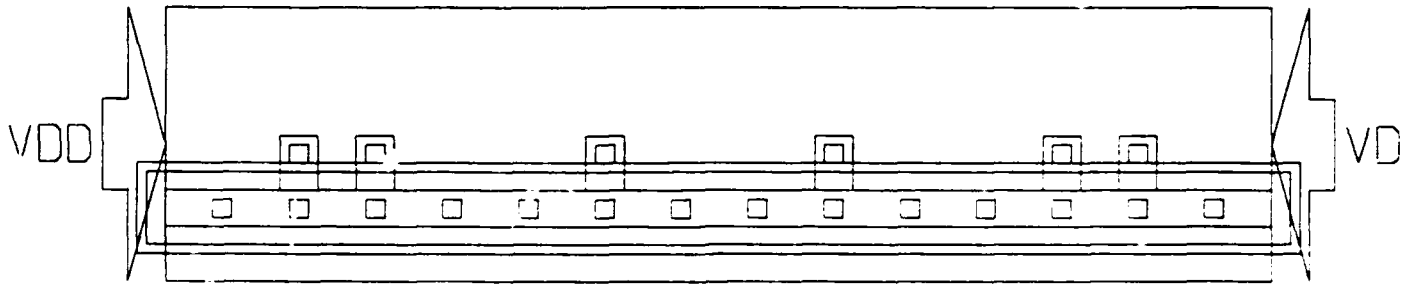
A. Transistor Specifications		
A.1 P Channel Transistor		
A.1.1 Treshold Voltage (50um/3.5um)	-0.90	+/- 0.2 V
A.1.2 Gamma (50um/50um)	0.57	+/- 0.05V^0.5
A.1.3 Ids Vds=5v, Vgs=-5v (50um/3.5um)	2.02	+/- 0.60 mA
A.2 N Channel Transistor		
A.1.1 Treshold Voltage (50um/3.0um)	0.90	+/- 0.2 V
A.1.2 Gamma (50um/50um)	1.0	+/- 0.05 V^0.5
A.1.3 Ids Vds=Vgs=5v (50um/3.0um)	6.3	+/- 1.8 mA
B. Sheet Resistances (Ohms per square)		
B.1 P+ Active (non-minimum island width)	112.5	+/- 62.5
B.2 N+ Active (non-minimum island width)	30	+/- 12
B.3 PWell (under field oxide)	5000	+/- 1000
B.4 Poly (In NDiff region)	30	+/- 20
C. Contact/Via String Resistance		
C.1 P+ Active to Metal Contact String	90	+/- 60
C.2 N+ Active to Metal Contact String	85	+/- 65

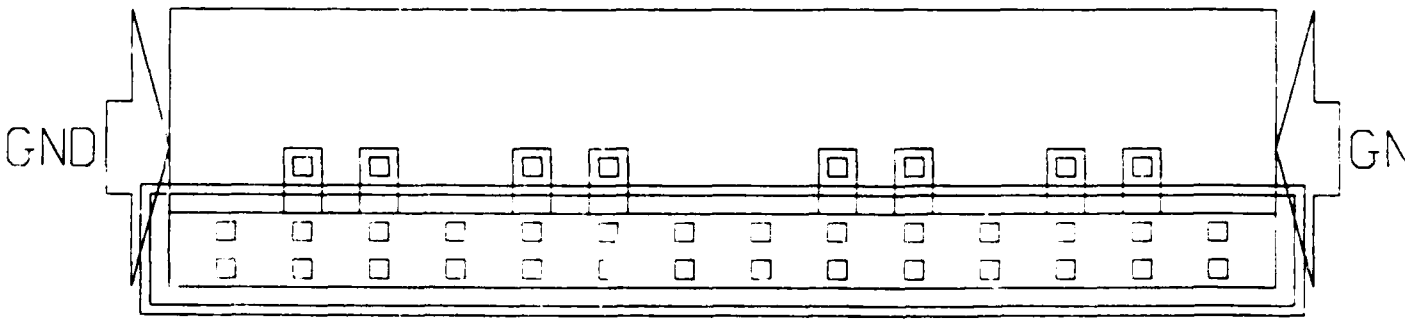
OVER



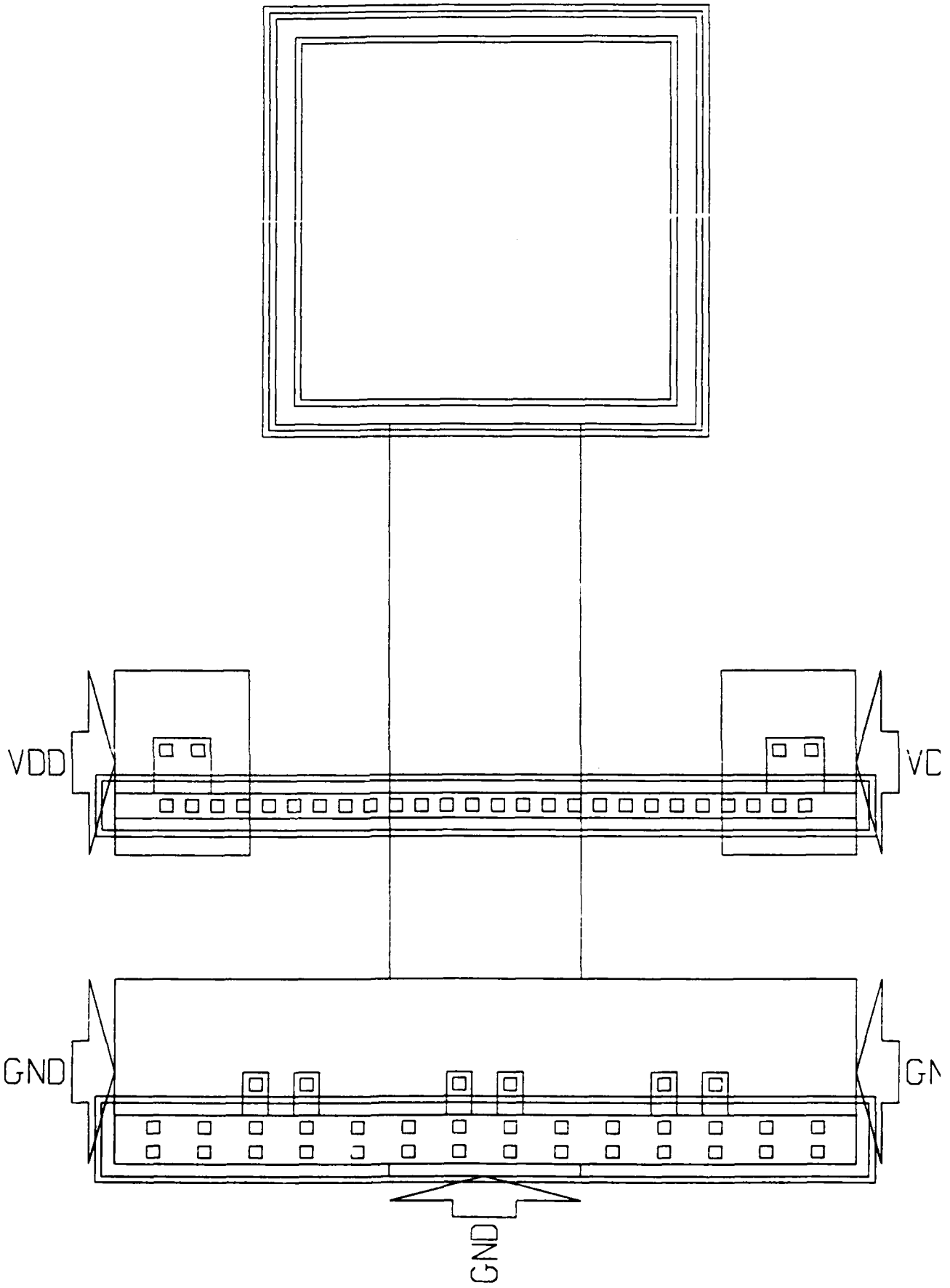
PADIO



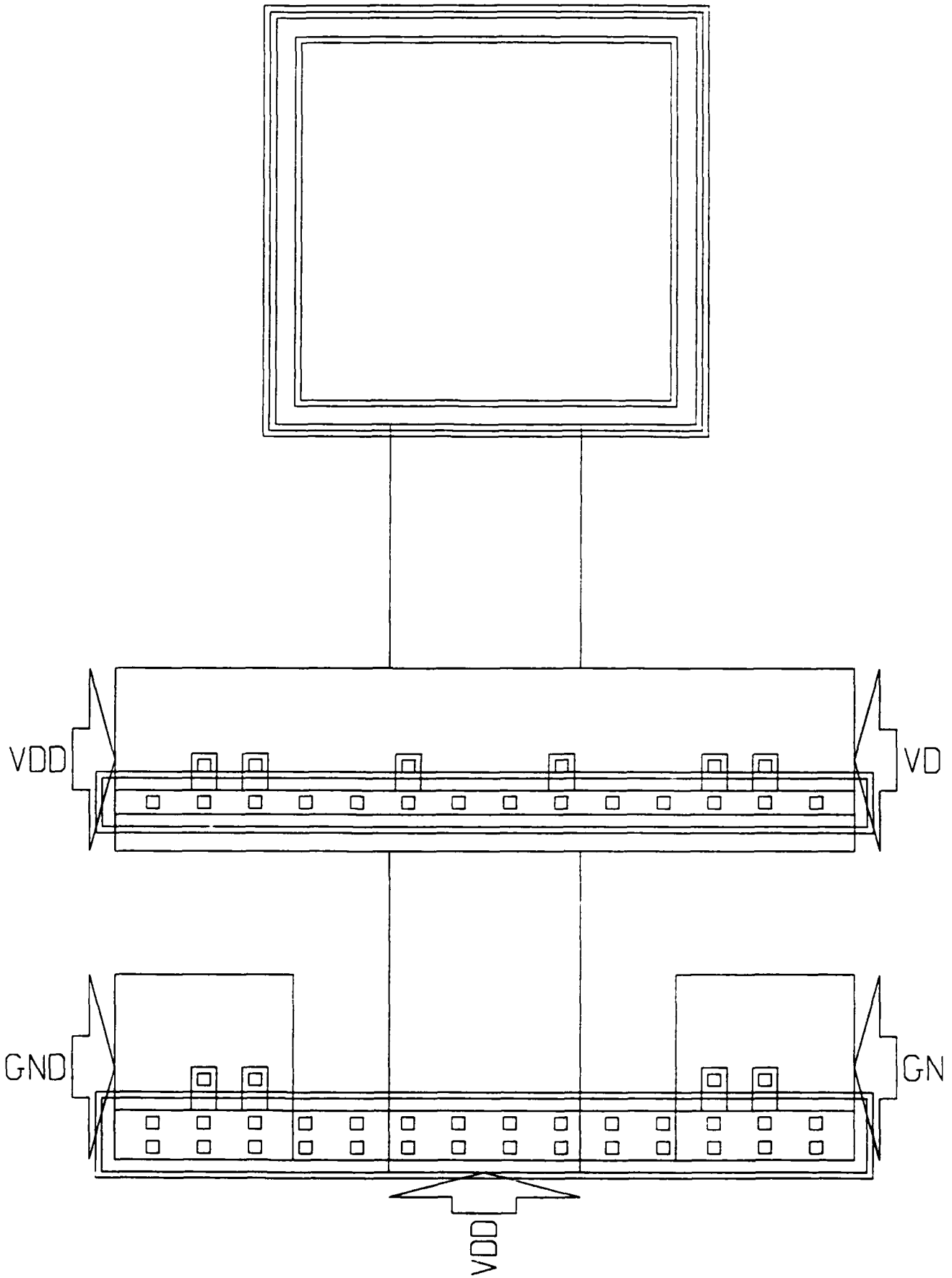




PADBLANK

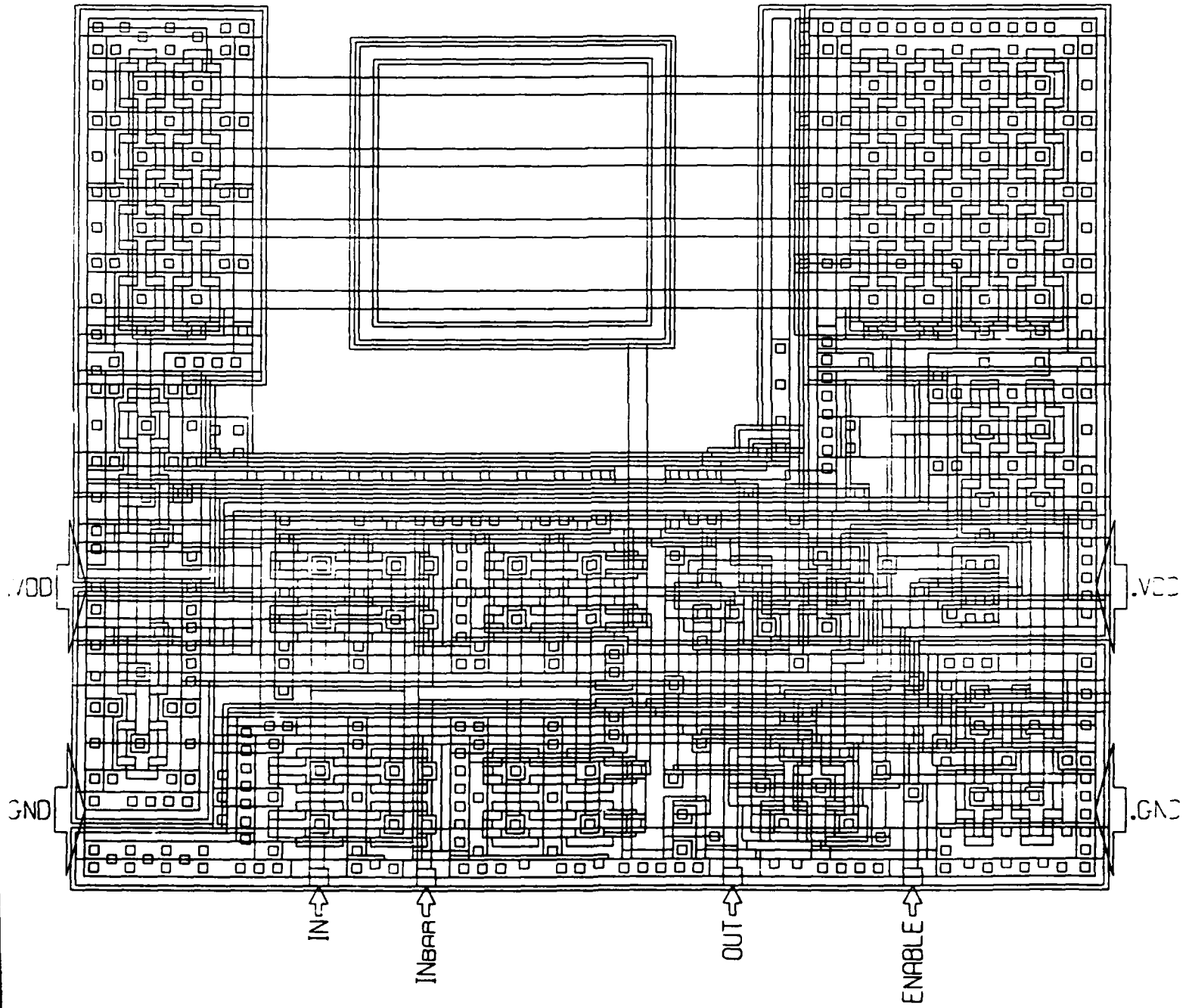


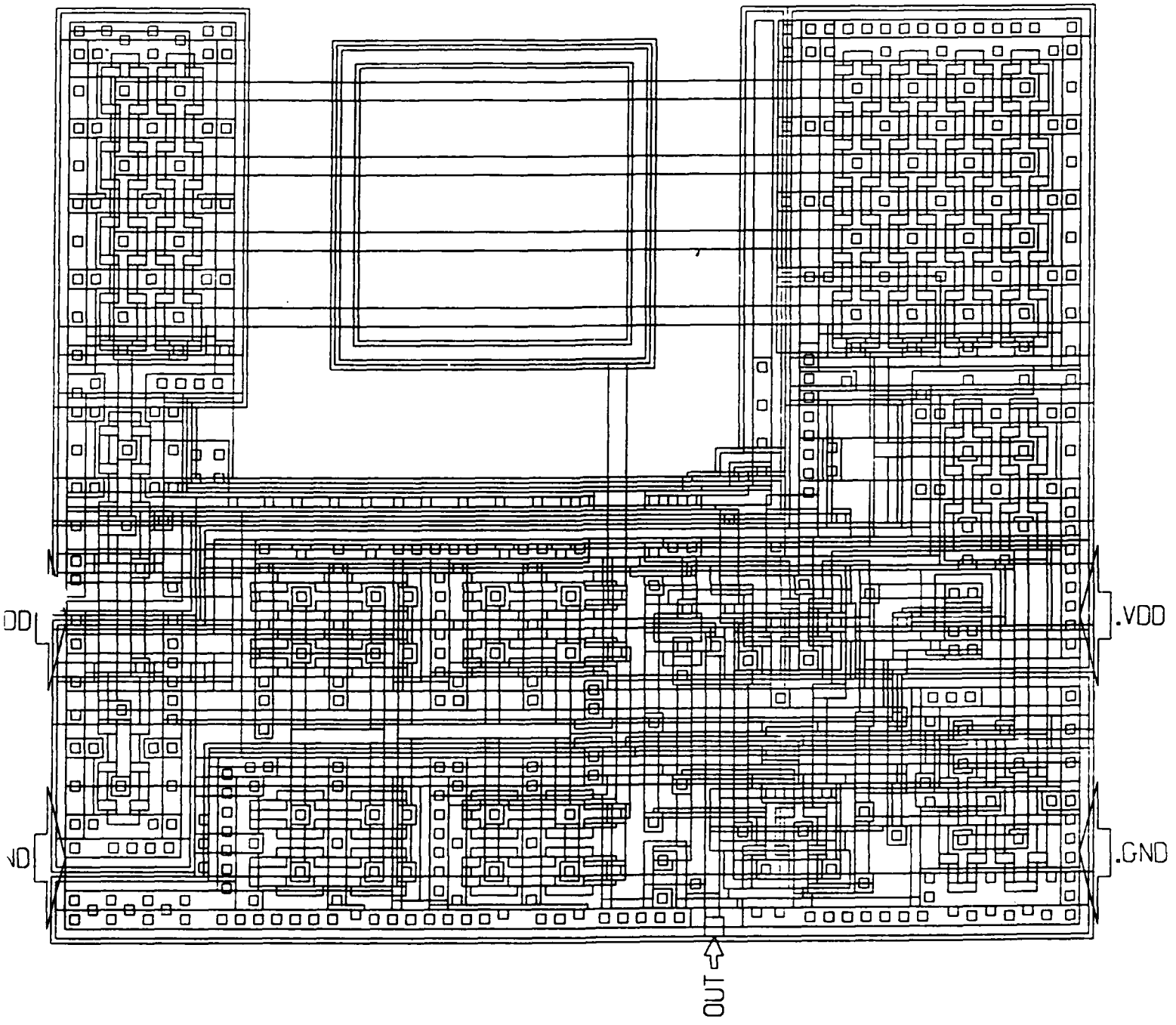
PADGND



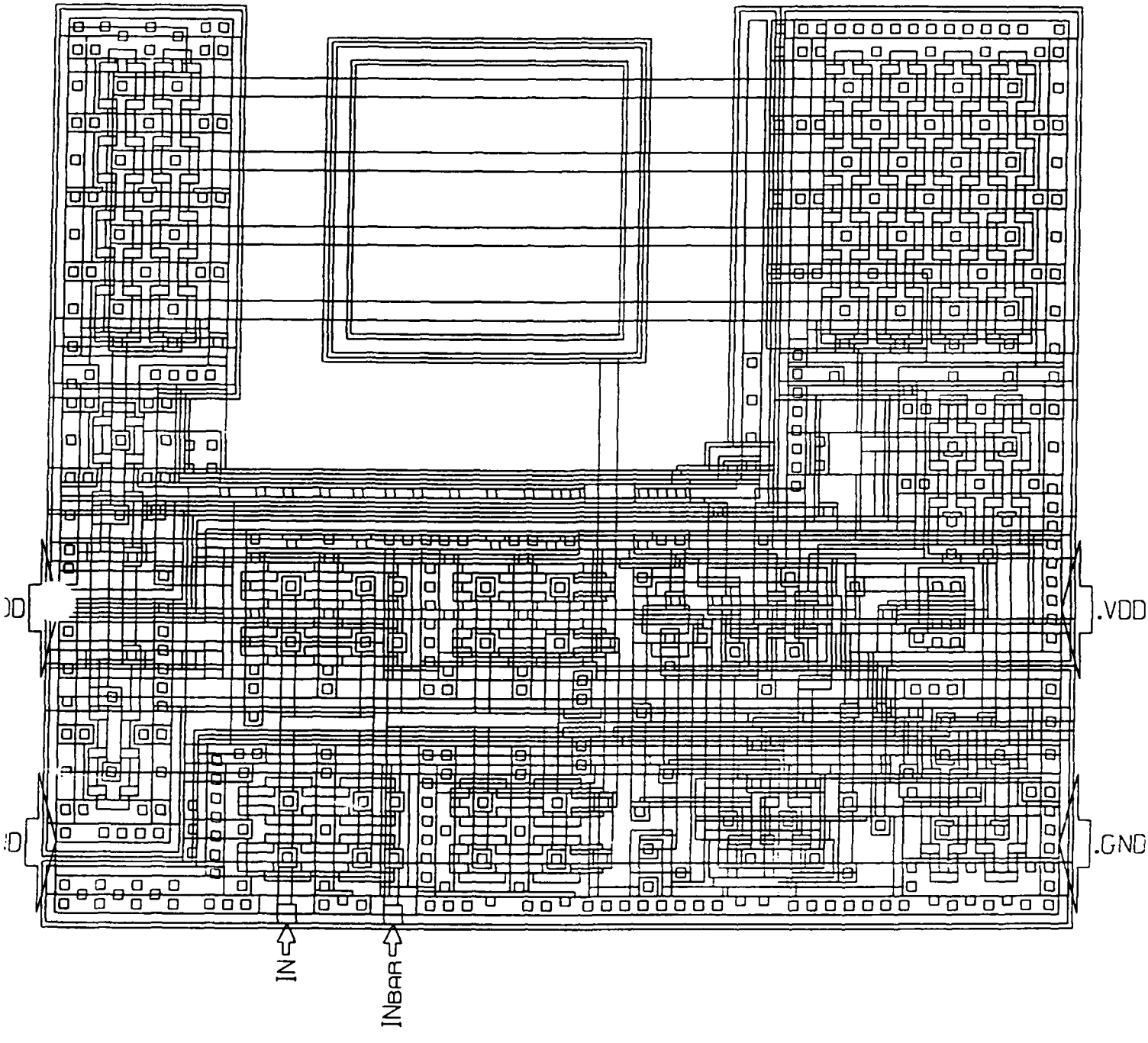
PADVDD

PADIO.CIF

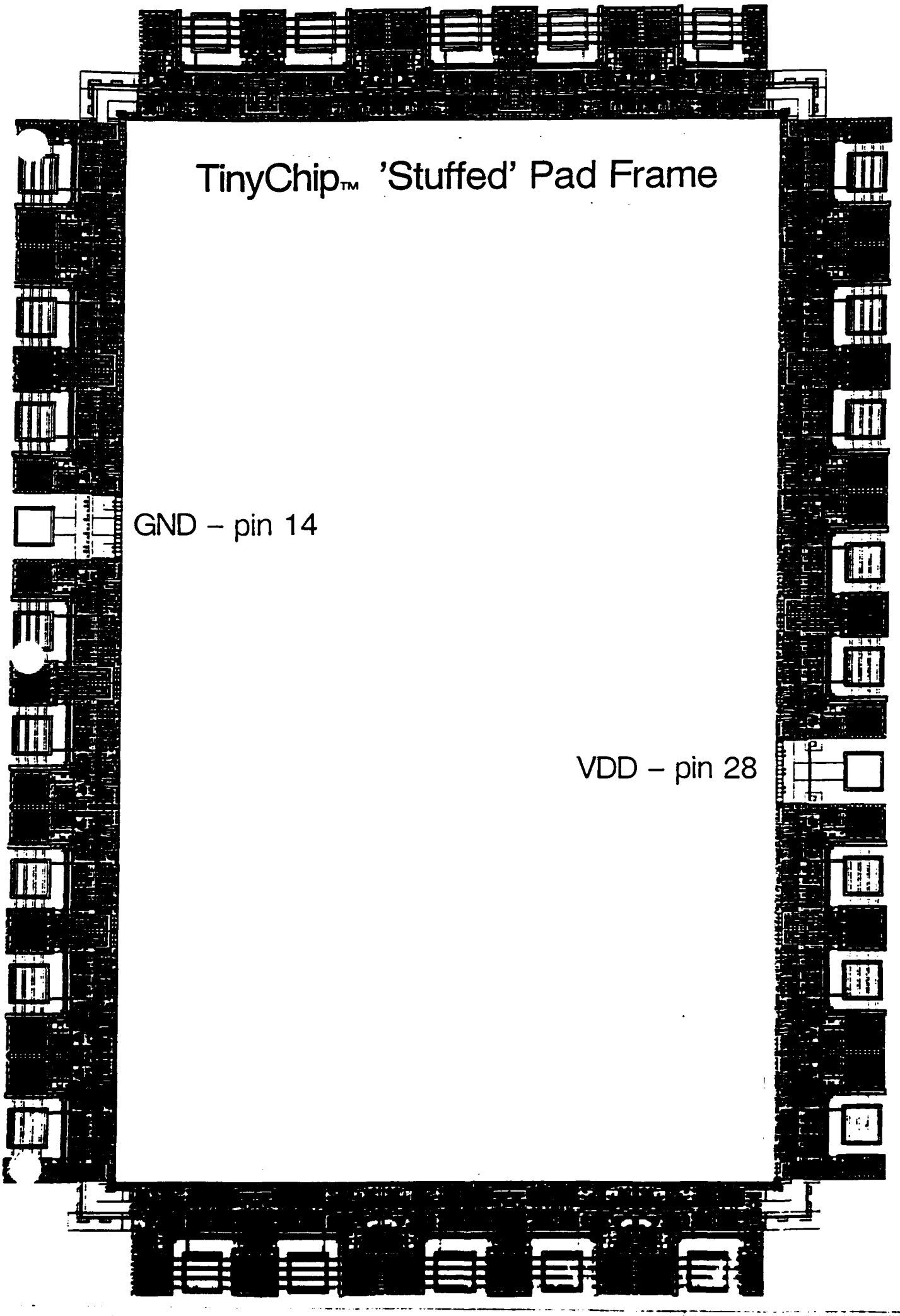




PADOUT

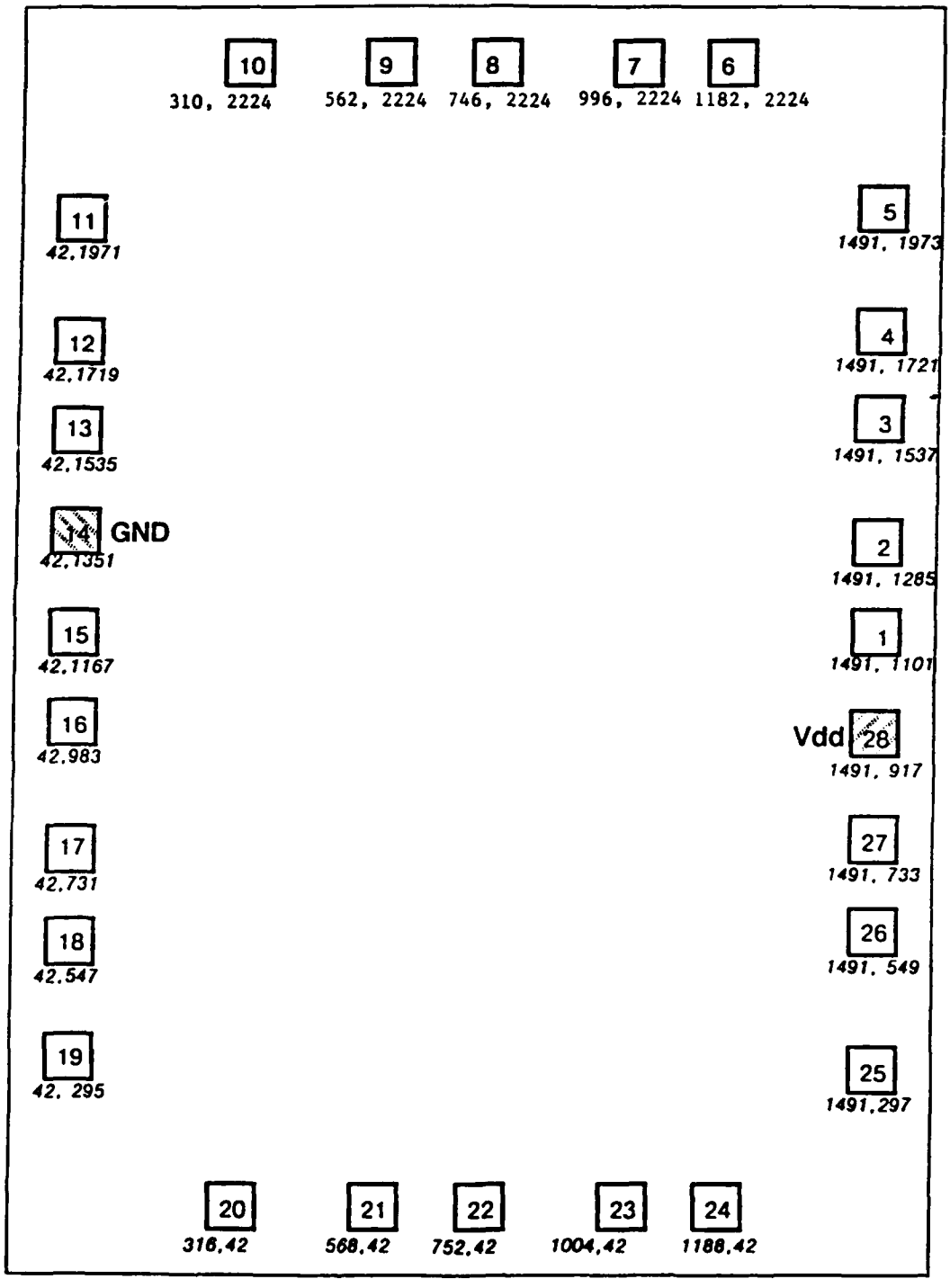


PADIN

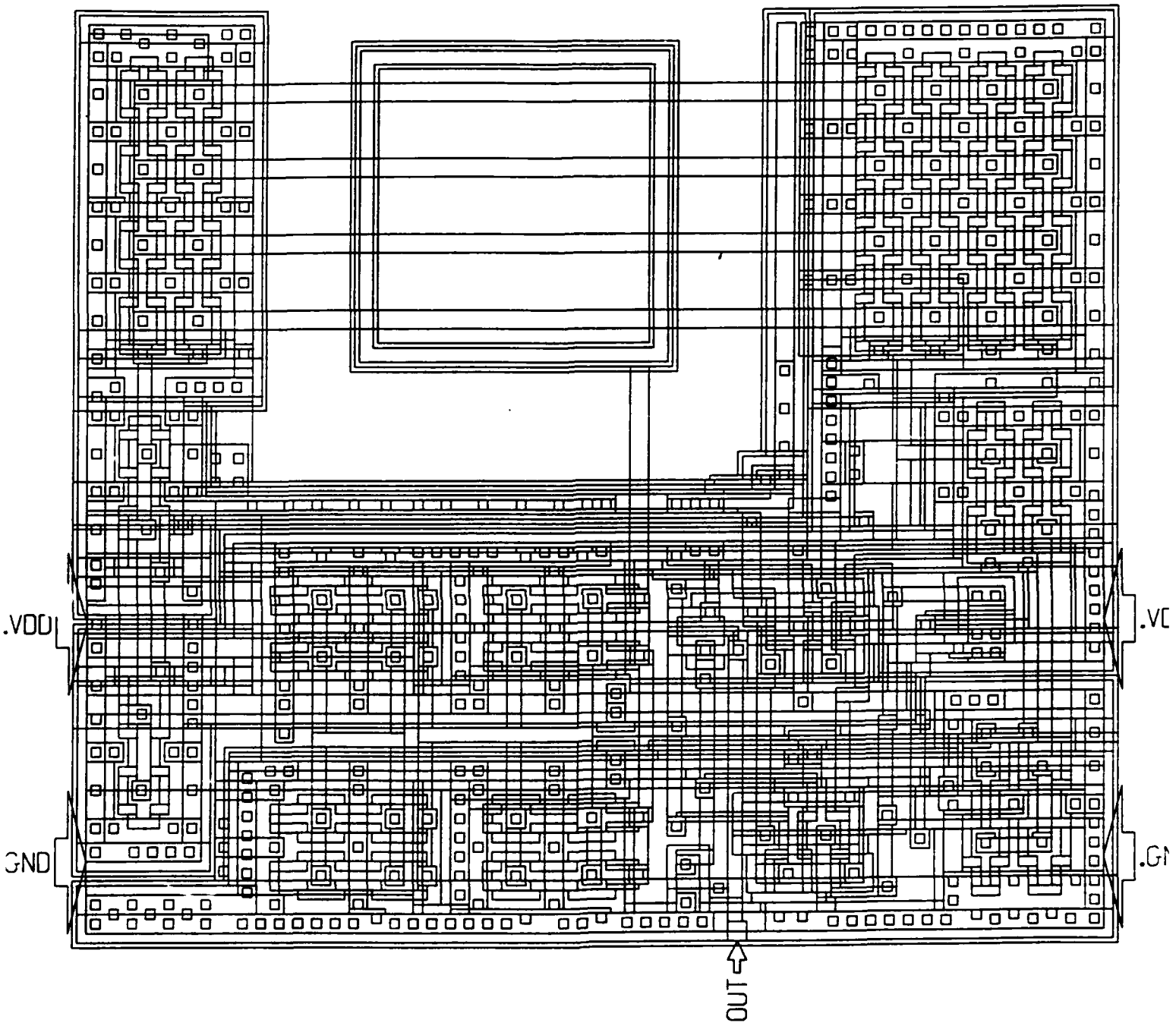

TinyChip™ 'Stuffed' Pad Frame
GND – pin 14
VDD – pin 28

3.0um TinyChip Standard Frame Pad Locations

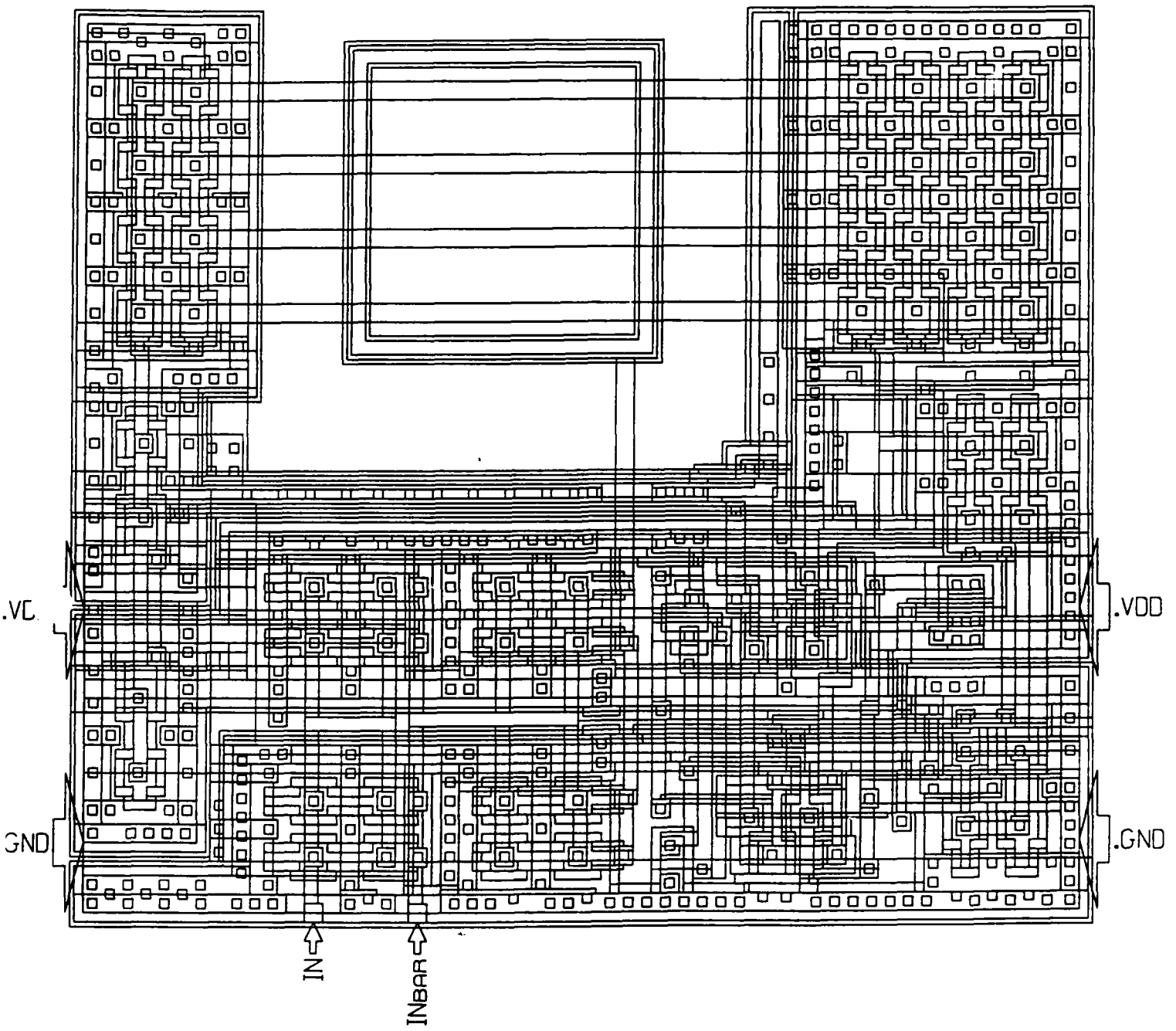
Pad Center Positions (in Lambda)



Size: 2300 x 3400 microns (1533 x 2266 Lambda)

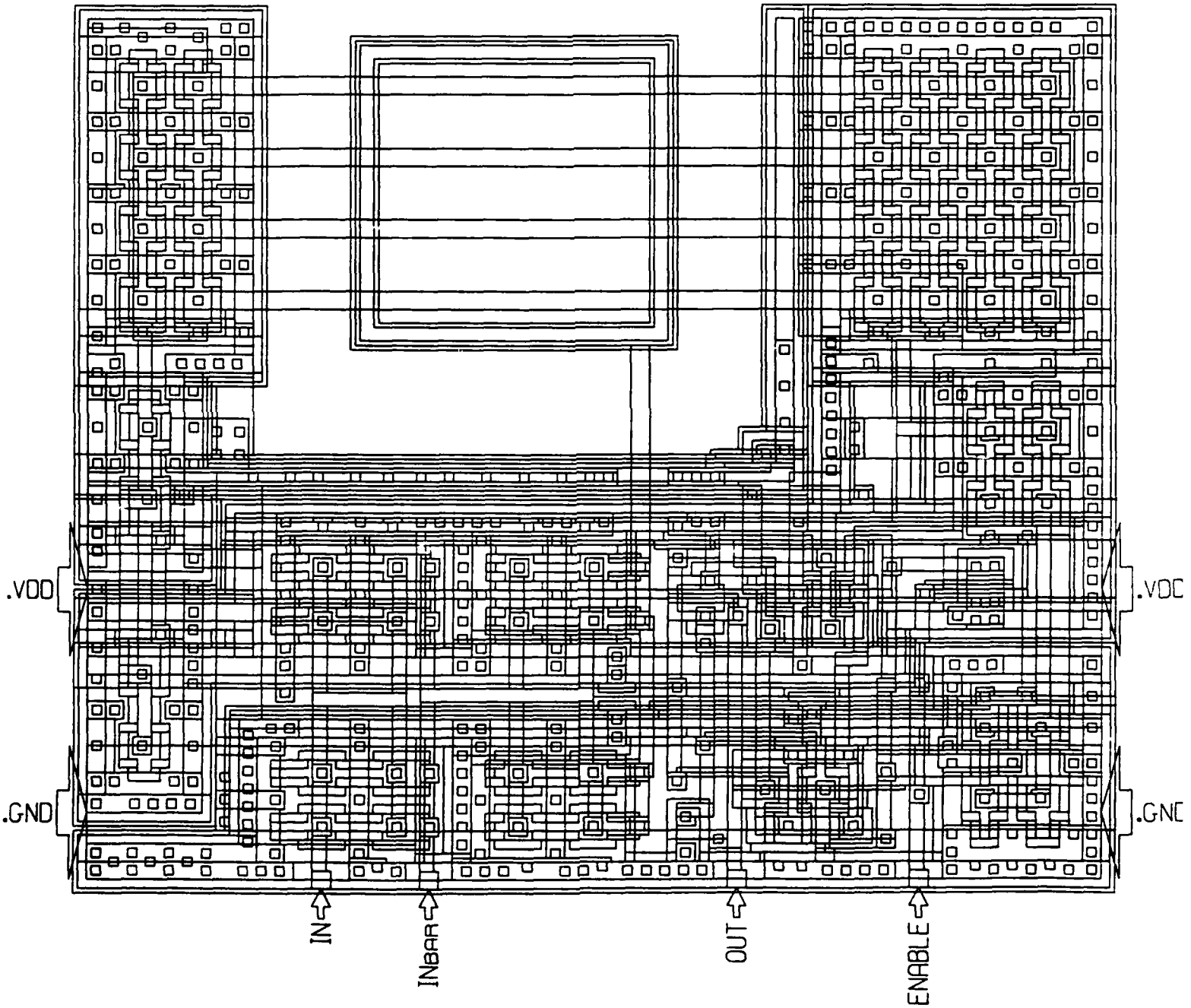


PADOUT



PADIN

PADIO.CIF



MOSIS – in 3 Steps

There are three basic steps to working with MOSIS – viewed from the perspective of you, the designer. They are 1) getting your paperwork processed 2) submitting your project and 3) receiving your packaged chips. Of course, steps 1 and 2 involve you intimately, while step 3 involves MOSIS and its vendors in the fabrication and packaging process.

Using MOSIS is not difficult but we know that you will have questions along the way. Feel free to contact the following MOSIS staff either via E–mail or at (310) 822–1511.

Order Information:	Kevin Stephens	STEPHENS@MOSIS.EDU
General Information	Sam Reynolds	SDREYNOLDS@MOSIS.EDU
Documentation Requests:	Wayne Tanner	TANNER@MOSIS.EDU

1

Customer Agreements and Purchase Order

MOSIS needs two signed copies of the MOSIS Customer Agreement form as well as a purchase order. To process your paperwork, MOSIS must receive a hardcopy purchase order one week prior to run–closing. If you require that a series of projects be fabricated over a period of time, MOSIS suggests setting up a blanket purchase order since this will be more efficient for your purchasing department.

2

Project Submissions

Please refer to the Technology Sheet in this packet for details on submitting your project to MOSIS. Note that geometry sent via E–mail needs to be received by MOSIS before 1:00 p.m. on the day the run closes. Magnetic tapes must be received at least 48 hours before the run–closing date. MOSIS cannot delay a run to wait for late designs.

3

Chip Fabrication and Delivery

On run–closing day, MOSIS collects all the projects of a particular technology and merges the designs onto a Multi–Project Wafer. After mask and wafer manufacturing and QA, MOSIS sends the wafer lot to the packager for wire bonding and assembly. Your packaged parts are then shipped to you by overnight mail – to the address specified on your purchase order.

Project Submission Form

1

Submitted by:

Name: _____

Phone Number: _____ Fax Number: _____

Mailing Address: _____

_____

_____

Account Number: _____

(must be included – call MOSIS at (310) 822-1511 if you're unsure of your account)

Purchase Order Number _____

(must be included if your project is going to be charged to a commercial account)

2

Indicate **one** of the following submission technologies:

SCMOS					CMOSN	VENDOR	
Lambda:____					Lambda:____	VTI_CMN20	HP_CMOS26B
SCP	SCE	SCNLC	SCN3M	SCNA	NSCN	ORBIT_CP	HP_CMOS34
SCN	SCPE	SCELC	SCE3M	SCEA	NSCP	ORBIT_CN	HP_AMOSI
	SCNE						
	SCEE				NSCE	VITESSE_HGAAS3	

3

Project Specifications:

MOSIS Project ID (if known):_____ Project Name: _____

Project Description: _____
(optional if commercial)

_____

Quantity (check one): Default ☐

Other ☐ If "other", specify total quantity desired. See the MOSIS price schedule for price and quantity guidelines. _____

Number of Pads: _____ Project Size (in Microns): _____

Is this a TinyChip project? ☐ Yes ☐ No

Do you want packaged chips? ☐ No ☐ Yes (indicate choice below)

☐ **Customer-Supplied Bonding Diagram (p. 3)** (not available on TinyChips)

☐ **Best Fit (calculated by MOSIS; diagrams shipped with packages)**

☐ **MOSIS Standard Frame** (specify frame name): _____

Check desired options: ☐ Substrate (not applicable to TinyChips)

☐ Hermetically Sealed Lids (not applicable to TinyChips)

☐ Foundry (specify:) _____

J92wt [illegible] options

4 **Tape Information:**

Record Length (default 2048 bytes/record): _____

Density (default 1600 BPI): _____

Data (Please check one):

☐ CIF ANSI ☐ CIF TAR ☐ CIF VMS_BACKUP ☐ GDSII STREAM ☐ MEBES PAM

5 **CIF Checksum:** _____ Byte Count: _____

6 **Top Structure / Library**

Top Structure Name (GDSII only): _____

Name of Referenced MOSIS Library
(e.g., CMOSN_30A): _____

7 **Layer Map**

☐ MOSIS default ☐ Other *(Please note: No layer merging or Boolean operations available.)*

Layer Name	GDS #	CIF Name	Layer Name	GDS #	CIF Name

8 **Authorization:**

Authorized Signature: _____

Name (Please Print): _____

Date: _____

MAIL THIS FORM WITH YOUR OFFLINE SUBMISSION TO:

SAM REYNOLDS
THE MOSIS SERVICE
4676 ADMIRALTY WAY
MARINA DEL REY, CA 90292-6695

CMOSN Library / MOSIS Documentation

Please refer to the MOSIS Price List and Order Form for the current prices of these items.

CMOSN Cell Library, Release 3.0A

This is a 2.0 and 1.2 micron scalable, double metal CMOS standard cell library developed by the DoD. It includes over 90 SSI and MSI-level macrocells with typical gate delays of less than 1ns, and up to 32K bits of RAM ROM. CMOSN was designed to meet high speed and high density random logic requirements as well as to provide maximum sourceability. Projects designed with this library (and the CMOSN design rules) can be submitted to MOSIS for fabrication. CMOSN distribution includes two cell notebooks with the logical, timing, etc. information, a magnetic tape with the layout of each cell, the RAM/ROM generator programs and a CMOSN Design rule set.

The distribution is available in both supported GDSII and unsupported CIF formats on a variety of media. Please refer to the MOSIS Price List and Order Form for details. **If you are ordering the library from us for the first time, we must receive a Cell Library Transfer Agreement signed by an authorized representative of your organization before we can send the library to you. If you do not have a Transfer Agreement, please call Wayne Tanner at (310) 822-1511 to obtain one. You can also FAX your request to his attention at (310) 823-5624.**

Note that if you are ordering Version 3.0A of the cell library and you have purchased a previous version from us, it is not necessary to sign another Transfer Agreement before receiving the update. Please indicate on the order form that a Transfer Agreement has already been signed and we will verify the information in our records on file.

CMOSN Cell Library Design Kit

The CMOSN library has also been loaded into various commercial CAD tools. Refer to the MOSIS Price List and Order Form for available vendors and formats. **Note that we must receive a Cell Library Transfer Agreement signed by an authorized representative of your organization before we can send the design kit to you. If you do not have a Transfer Agreement, please call Wayne Tanner at (310) 822-1511 in order to obtain one. You can also FAX your request to his attention at (310) 823-5624.**

NOTE: It is suggested that MAGIC users look into utilizing the Institute for Technology Development's version of this library. For more information, contact Dan Johnson at (601) 932-7620 or e-mail at danj@aue.com.

The MOSIS User Manual

The *MOSIS User Manual* includes chapters on how to get started with MOSIS, becoming a MOSIS User, CMOS technologies, MOSIS libraries, compatible VLSI CAD tools, packaging and bonding, quality control and other services.

Technical Information Packet

This diskette contains wafer acceptance and general process specifications for MOSIS CMOS vendors: Orbit 2um and Orbit 2um Low Noise Analog, VLSI 2um, and Hewlett-Packard 1.2 and 0.8um processes. It also contains available vendor-provided SPICE parameters for these process technologies as well as MOSIS measured parameters and SPICE for specific runs (wafer lots).

Pad Libraries Packet

This packet includes a diskette containing CIF and GDSII pad layout and documentation files for all MOSIS pad libraries, including the TinyChip and TinyChip pad libraries.

MOSIS Price List and Order Form

FABRICATION

ITEM #	DESCRIPTION	UNIT	Standard Unit Price	Discount* Unit Price	# OF UNITS	TOTAL PRICE
1. CMOS 2 MICRON (priced per lot – includes packaging):						
10011	2.22 x 2.25 mm or smaller (Tiny)	Lot of 4	$520	$480		
10011	Additional quantities of #10011 above	Lot of 4	$520	$480		
10007	4.6 x 6.8 mm or smaller (Small)	Lot of 12	$2,600	$2,410		
10008	Additional quantities of #10007 above	Lot of 8	$1,690	$1,560		
10003	6.9 x 6.8 mm or smaller (Medium)	Lot of 24	$6,150	$5,640		
10004	Additional quantities of #10003 above	Lot of 8	$2,030	$1,860		
10001	7.9 x 9.2 mm or smaller (Large)	Lot of 32	$11,900	$10,860		
10002	Additional quantities of #10001 above	Lot of 8	$2,960	$2,700		
2. CMOS ANALOG 1.2 MICRON (priced per lot – includes packaging):						
10123	2.1 x 2.1 mm or smaller (Tiny)	Lot of 5	$950	$900		
	Additional quantities of #10123 above	Lot of 5	$950	$900		
10124	4.5 x 4.5 mm or smaller (Small)	Lot of 10	$3,730	$3,550		
	Additional quantities of #10124 above	Lot of 10	$3,730	$3,550		
10125	9.3 x 9.3 mm or smaller (Large)	Lot of 20	$14,240	$13,540		
	Additional quantities of #10125 above	Lot of 20	$14,240	$13,540		
3. 5X RETICLE RUNS (priced per SQ MM – does not include packaging):						
10121	1.2 micron CMOS-5X (25 parts)	sq mm	$450	$380		
10122	Additional 25 parts of #10121 above	sq mm	$350	$290		
10119	0.8 micron CMOS-5X (25 parts)	sq mm	$550	$480		
10120	Additional 25 parts of #10119 above	sq mm	$420	$370		
10117	HGaAs3-5X (20 parts)	sq mm	$580	$530		
10118	Additional 20 parts of #10117 above	sq mm	$450	$410		

Minimum die size for 1.2 and 0.8 processes is 1.94 x 1.94 mm, and 2.16 x 2.45 mm for GaAs. Please calculate in microns, converting result to square millimeters carried out to three decimal places. The price should be rounded to the nearest dollar. For example, a sample minimum charge calculation for a 1.2 micron project is:

(1.94 mm) * (1.94 mm) = 3.764 sq.mm ; [(3.764 sq.mm) * ($450 / sq.mm)] = $1,694

Note that any packaging charges are added to this base figure (see packaging costs in next column).

PACKAGING

ITEM #	DESCRIPTION	UNIT	Standard Unit Price	Discount* Unit Price	# OF UNITS	TOTAL PRICE
4. CMOS-5X PACKAGING						
DIP28	28-pin DIP	ea	$20	$19		
DIP40	40-pin DIP	ea	$20	$19		
PGA65	65-pin PGA	ea	$40	$37		
PGA84	84-pin PGA	ea	$40	$37		
PGA108	108-pin PGA	ea	$40	$37		
PGA132	132-pin PGA	ea	$40	$37		
5. HGaAs3-5X PACKAGING						
PGA149	149-pin PGA	ea	$130	$120		
PGA211	211-pin PGA	ea	$160	$150		
LDCC28	28-LDCC	ea	$50	$50		
LDCC52	52-LDCC	ea	$70	$70		
LDCC132	132-LDCC	ea	$140	$130		
LDCC164	164-LDCC	ea	$140	$130		
LDCC256	256-LDCC	ea	$210	$200		
LDCC344	344-LDCC	ea	$270	$260		
6. MISCELLANEOUS PACKAGING						
CUSTDIP	Customer-supplied DIP	ea	$20	$17		
CUSTPGA	Customer-supplied PGA	ea	$40	$36		
CUSTLDCC	Customer-supplied LDCC	ea	$60	$53		

Subtotal for Page 1

continued

Prices valid from July 1, 1993 through December 31, 1993

*The discounted price is available to Universities, Government Agencies and Organizations ordering work that will be charged to a government contract. To qualify for this discount, you must include the following information on your purchase order: (1) funding agency; (2) contract number; (3) government program manager; and (4) contract expiration date.

MOSIS CUSTOMER AGREEMENT
(Government Purchaser)

This Agreement is made this the ____ day of _____, 19__ by and between the UNIVERSITY OF SOUTHERN CALIFORNIA, a California non-profit corporation, acting through its Information Sciences Institute, located at 4676 Admiralty Way, Marina del Rey, California 90292-6695 (hereinafter referred to as "USC/ISI"), and:

_____
Customer/Organization

_____
Department

_____
Street Address

_____
City, State and Zip Code

_____
Area Code and Phone Number

(HEREINAFTER referred to as "Customer".)

RECITALS

WHEREAS, USC/ISI has developed a computerized system which provides integrated circuit fabrication services through third party vendors to commercial users (hereinafter referred to as "MOSIS"); and

Customer desires to have USC/ISI provide them with such services,

NOW, THEREFORE, in consideration of the covenants and conditions contained herein, the parties agree as follows:

1. TERM

Customer shall submit to USC/ISI a purchase order(s) for MOSIS services which shall be subject to written acceptance by USC/ISI and shall only be effective upon such acceptance; all such purchase order(s) shall specify the dollar amount of services desired by Customer.

2. SERVICE

a. USC/ISI shall utilize the MOSIS service to: (1) check that syntax is correct (but not including design validation) and deliver wafers or a set of bonded and packaged integrated circuits (chips) containing the design as submitted by Customer; and (2) provide fabrication of prototype quantities of integrated circuits.

b. Circuits shall either be bonded per Customer instructions or Customer shall be provided with a diagram showing how bonding was done. Individual parts shall be inspected but shall not be tested. Spice parameters, which have been extracted from USC/ISI devices on the same run, shall be provided to Customer.

c. Each fabrication run shall have passed the vendors' quality assurance process and shall have been tested to ensure that it has conformed to MOSIS fabrication requirements. Details are technology specific and are available upon request.

3. RATES

Charges to Customer shall be set forth in an attached purchase order, the terms of which are fully incorporated herein by this reference. Such purchase order shall be approved in writing by USC/ISI by means of an authorized signature of USC/ISI appearing on said purchase order.

4. NO WARRANTIES

Customer expressly recognizes that the ability of the MOSIS services to provide working parts in a consistent manner is speculative. USC/ISI EXPRESSLY DISCLAIMS ANY WARRANTY THAT USE OF THE MOSIS SERVICES WILL PROVIDE WORKING OR USABLE PARTS, AND CUSTOMER IS NOT RELYING ON ANY WARRANTY OR ON ANY UNDERSTANDING OR BELIEF THAT USE OF THE MOSIS SERVICES WILL PROVIDE WORKING OR USABLE PARTS, AND UNDERSTANDS AND ACCEPTS THAT EACH FABRICATION USING THE MOSIS SERVICES PROVIDED BY USC/ISI SHALL BE ON AN "AS IS" BASIS. USC/ISI EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES AND THERE ARE NO WARRANTIES THAT EXTEND BEYOND THE

DESCRIPTION ON THE FACE HEREOF. USC/ISI SHALL NOT BE RESPONSIBLE FOR ANY DIRECT, INDIRECT, INCIDENTAL OR CONSEQUENTIAL DAMAGES CUSTOMER MAY SUFFER RELATING TO THE USE OF ANY MOSIS FABRICATION. USC/ISI MAKES NO WARRANTIES, EITHER EXPRESS OR IMPLIED, AS TO ANY MATTER WHATSOEVER, INCLUDING WITHOUT LIMITATION, THE CONDITION OF THE FABRICATION, ITS MERCHANTABILITY OR ITS FITNESS FOR ANY PARTICULAR PURPOSE. USC/ISI shall not be liable for, and Customer hereby assumes the risk of, and will release ad forever discharge USC/ISI, its agents, officers, and employees, either in their individual capacities or by reason of their relationship to USC/ISI, with respect to any expense, claim, liability, loss, or damage (including any incidental or consequential damage), either direct or indirect, whether incurred, made or suffered by Customer or by any third parties, in connection with or in any way arising out of the furnishing or use of the MOSIS fabrication. In any event, USC/ISI's liability to Customer on any ground whatsoever shall not exceed a sum equal to the fee paid to USC/ISI by Customer hereunder.

5. CONFIDENTIALITY AND PROPRIETARY RIGHTS

a. Both parties recognize that the information exchanged hereunder is of a confidential and proprietary nature. USC/ISI shall maintain all such confidential and proprietary information provided by Customer hereunder in confidence. As this Agreement envisions transfer of such information to third party vendors, USC/ISI agrees that it shall require each such vendor to execute a Nondisclosure Agreement which shall extend to the information provided by Customer and which shall provide for an obligation of confidentiality commensurate with the obligation called for in this Agreement. USC/ISI further agrees that it shall treat Customer's confidential and proprietary information with the same care with which it treats its own confidential and proprietary information. The obligation of confidentiality shall extend for a period of five (5) years from the date of disclosure by Customer to USC/ISI and, to that extent, this obligation shall survive termination of this Agreement.

b. Customer recognizes, however, that because of circumstances beyond the direct control of USC/ISI, there may be disclosure of the material to third parties. USC/ISI, however, shall not be liable for any negligent disclosure of Customer's material by any USC/ISI employee or agent, or by any third party vendor, except as otherwise provided for herein.

c. Notwithstanding the provisions of paragraph 5(a), USC/ISI shall not be obligated with respect to any information which: (i) at the time of disclosure has been published or otherwise is in the public domain; and/or (ii) after disclosure is published or otherwise becomes a part of the public domain through no fault of USC/ISI; and/or (iii) is or has been rightfully disclosed to USC/ISI by a party that has no obligation to Customer, directly or indirectly, with respect thereto to the extent that any such third party disclosure is received by USC/ISI without an obligation of confidentiality.

d. Customer specifically agrees that it shall not disclose any material which may be considered proprietary or confidential material of USC/ISI or of any vendors to any third parties. Proprietary material shall include but shall not be limited to, proprietary vendor information such as yield and parametric data, whether it was provided to Customers or extracted by them. USC/ISI agrees that it shall mark its own technical data and proprietary software in accordance with the provisions of DFARS 52.227-7013. Customer agrees that it shall be precluded by 18 U.S.C. 1905 and any and all other appropriate laws and regulations from knowingly divulging the trade secrets of USC/ISI, and/or any third party vendor.

e. Customer shall be furnished with a list of vendors; if Customer wishes, Customer shall have the opportunity to prohibit certain vendors from working on its fabrication. Vendors shall have been provided with a list of Customers and shall also have the opportunity to refuse to work on the fabrications of certain Customers. USC/ISI shall not knowingly provide to any vendor which the Customer desires to prohibit from

working on its fabrication any confidential/proprietary information of Customer.

f. Nothing in this Agreement shall serve to convey to USC/ISI any proprietary rights in any design submitted by Customer pursuant to this Agreement or in any semi-conductor chip fabricated therefrom. All rights, titles and interests in and to designs for integrated circuits submitted by Customer pursuant to this Agreement as well as all mask works fixed or embodied in any semi-conductor chip fabricated pursuant to this Agreement shall belong entirely to Customer to the extent that Customer has such rights, titles and interests prior to submission to USC/ISI. USC/ISI shall not be responsible for securing any form of statutory protection, whether by patent, copyright, registration under the Semi-Conductor Chip Protection Act, or otherwise unless a separate signed written agreement between Customer and USC/ISI is entered into upon such terms and conditions as the parties may agree upon.

g. Customer agrees that it would be difficult and impractical, if not impossible to calculate the dollar amount of damages which might result from the disclosure by USC/ISI, or any employee or agent thereof, or by any third party of Customer's or any employee or agent thereof of any confidential and/or proprietary information.

CUSTOMER THEREFORE AGREES THAT USC/ISI'S TOTAL LIABILITY FOR SUCH DISCLOSURE SHALL BE LIMITED TO THE AMOUNT PAID BY CUSTOMER TO USC/ISI UNDER THE TERMS OF THIS AGREEMENT AND THAT SAID AMOUNT IS REASONABLE COMPENSATION FOR SUCH DAMAGES.

6. SEVERABILITY

If any part, term or provision of this Agreement shall be held illegal, unenforceable or in conflict with law of a federal, state or local government having jurisdiction over this Agreement, the validity of the remaining provisions shall not be affected thereby.

7. MISCELLANEOUS

a. The parties agree to abide by all applicable federal, state and local laws and regulations which regulate the activities envisioned by this Agreement.

b. This Agreement together with any signed attachments thereto, contains all of the agreements, representations, and understanding of the parties hereto and supersedes any previous understandings, commitments, or agreements, oral or written. Any modification to this Agreement must be in writing and signed by both parties.

IN WITNESS WHEREOF, the parties hereto have set their hand.

UNIVERSITY OF SOUTHERN CALIFORNIA, INFORMATION SCIENCES INSTITUTE	_____ (Customer/Organization)
By: _____ (Signature)	By: _____ (Signature)
_____ (Type or print name)	_____ (Type or print name)
Date: _____	Date: _____

APPLICATION FOR ACCESS TO ARPA / NSF SILICON BROKERAGE SERVICE (MOSIS) TO SUPPORT RESEARCH AND GOVERNMENT AGENCIES

The National Science Foundation (NSF) and the Advanced Research Projects Agency (ARPA) are providing access to the ARPA/NSF Silicon Brokerage Service (MOSIS) to principal investigators of ARPA and NSF supported research programs, for fabrication of VLSI chips and printed circuit boards relating to the supported research.

BACKGROUND

As part of ARPA's research in the VLSI area, they have developed a capability called MOSIS for fast turnaround fabrication of small quantities of custom VLSI chips. MOSIS is a brokerage service which aggregates the needs of a large design community and represents them to the U.S. semiconductor industry through a single interface.

Designs are submitted to MOSIS in digital form over electronic mail using standard design rules and standard artwork formats CIF or UU-Encoded GDS. The integrated circuits are fabricated at selected foundries, packaged and sent to the designer within a few weeks of submission to MOSIS.

The MOSIS service is located at the Information Sciences Institute of the University of Southern California (USC/ISI) located in Marina del Rey, California.

TERMS AND CONDITIONS

1. The principal investigator must provide a brief report to MOSIS for each fabricated project. This report must be submitted within three months after receipt of the packaged chips and will contain:

   a. Number of dies received

   b. Number tested for functionality

   c. Number that were functional

   d. Remarks (design errors, processing errors, errors of unknown source)

2. Users will be required to comply with all operating rules governing use of MOSIS. These will be communicated to successful applicants.

3. ARPA and NSF reserve the right to limit use by individuals and institutions.

4. Neither NSF, ARPA or USC/ISI assume responsibility or liability for the units produced or the time required to produce them.

5. MOSIS will fabricate designs exactly as submitted. MOSIS will check that the layout file syntax is correct but will not validate designs.

6. Designers specifically agree that they shall not disclose any material which may be considered proprietary or confidential material of USC/ISI or of any vendors to any third parties. Proprietary material shall include, but shall not be limited to, proprietary vendor information such as yield and parametric data, whether it was provided to customers or extracted by them.

SUBMISSION OF APPLICATION

Attached is an application form which must be submitted to MOSIS by all organizations who are requesting government-sponsored access to MOSIS.

1. ORGANIZATIONS WITH ARPA CONTRACTS OR NSF GRANTS who wish to use MOSIS for work performed under the contract or grant must attach a copy of the MOSIS application to their original proposal to DARPA or NSF.

2. GOVERNMENT AGENCIES AND ORGANIZATIONS WITH GOVERNMENT CONTRACTS (not sponsored by ARPA or NSF) can work with MOSIS in one of two ways:

   a. They can purchase services directly from MOSIS.

   b. Government agency (or sponsoring agency) may be able to transfer funds through ARPA to cover the cost of fabrication. These MOSIS accounts will be activated when the funds have been received by ARPA.

3. UNIVERSITIES TEACHING VLSI DESIGN CLASSES who wish to apply for NSF-sponsorship should get a special application from MOSIS.

4. ALL OTHER ORGANIZATIONS can send a purchase order along with each submitted design. Note that MOSIS must have a signed customer agreement before purchase orders can be accepted. For more information, contact Kathleen Fry at (310)822-1511 or <FRY@MOSIS.EDU>.

The attached application is to be submitted to the following address:

THE MOSIS SERVICE - PROPOSALS
USC INFORMATION SCIENCES INSTITUTE
4676 ADMIRALTY WAY
MARINA DEL REY, CA 90292-6695

Note that applications must have a separate page 3 for each government fiscal year of the proposed work.

AMOUNT OF AWARD

Successful applicants will be given a MOSIS account which includes a budget for the amount of the award.

ARPA awards will be made according to the government fiscal year (October through September). NSF awards will be according to the university fiscal year (July to June).

The attached application form is to be used to estimate the cost of an applicant's fabrication requirement. The amount of the award will be based on (1) the applicant's estimate and (2) the amount of funds available from NSF or ARPA.

If an organization's need for fabrication exceeds the amount of award, services can be purchased directly from MOSIS. Contact Kathleen Fry at (310) 822-1511 or < FRY@MOSIS.EDU > for more information.

ADDITIONAL INFORMATION

Descriptions of new design methodologies which simplify VLSI system design are contained in the books *Introduction to VLSI Systems* by Mead and Conway (Addison-Wesley 1981); *Principles of CMOS VLSI Design, A Systems Perspective* by Neil Weste and Kamran Eshraghian; and the report "A Guide to LSI Implementation" by Hon and Sequin (second edition, Xerox Palo Alto Research Center).

Attachments: Application to Use ARPA/NSF Silicon Brokerage Service for Research
MOSIS Fabrication Schedule
MOSIS Design Rules: Scalable CMOS/Bulk

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Application to Use ARPA/NSF Service (MOSIS)
for Fabrication of Prototype Quantities of Custom Integrated Circuits
to Support Research

1. General Information (Please type or print)

Name: _____ _____

Organization: _____

Department: _____

Mailing Address: _____

_____

_____

Phone Number: _____

Network Address: _____

2. Contract / Grant Information

Contract or Grant Number: _____

Total Amount of Award or Proposal: _____

Period of Performance: _____ **through** _____

Principal Investigator: _____

Sponsoring Agency: _____ _____

Program Manager: _____ _____

Title of the Project: _____

ARPA Order Number: _____ **(if ARPA-sponsored)**

3. Abstract of Program

(continued)

Attachments: **Background and qualifications of key personnel**
Narrative (not to exceed four double-spaced pages)

**Application to Use ARPA/NSF Service (MOSIS)
for Fabrication of Prototype Quantities of Custom Integrated Circuits
to Support Research**

3. Abstract of Program (continued)

4. Equipment Access

What hardware and software are you using for design, simulation and testing?

_____

_____

_____

5. Signature

I agree to provide a brief report to USC/ISI after each fabricated project is received. This report will be submitted within three months after receipt of circuits and will contain the following information:

1. **Number of chips received**
2. **Number tested for functionality**
3. **Number of functional parts**
4. **Remarks (include design and processing errors, etc.)**

I understand that neither NSF, ARPA or USC/ISI assumes responsibility or liability for the units produced or the time required to produce them and that NSF and ARPA jointly reserve the right to limit use by individuals and institutions. I agree to comply with all rules governing use of the service, including protection of confidential information.

I also understand that MOSIS will fabricate my design exactly as submitted and that MOSIS will check that the layout file is correct but will NOT validate my design.

I certify that 1) I have access to an electronic communications network and I can submit projects to MOSIS electronically in either CIF or UU-Encoded GDS format, and 2) I have access to equipment and software that is adequate for designing, simulating and testing integrated circuits.

Authorized Signature: _____

Name (please type): _____

Title: _____

Date: _____

The MOSIS Service *(310) 822-1511*
Information Sciences Institute *4676 Admiralty Way* *Marina del Rey, CA 90292-6695*

PART #	DESCRIPTION	UNIT	UNIT PRICE	# OF UNITS ORDERED	TOTAL PRICE
1. CMOS 2 micron (priced per lot – includes packaging):					
10011	2 micron CMOS, 2.22 x 2.25 mm or smaller	Lot of 4	$440		
"	Additional quantities of part #10011 above	Lot of 4	$440		
10007	2 micron CMOS, 4.6 x 6.8 mm or smaller	Lot of 12	$2,210		
10008	Additional quantities of part #10007 above	Lot of 8	$1,430		
10003	2 micron CMOS, 6.9 x 6.8 mm or smaller	Lot of 24	$5,120		
10004	Additional quantities of part #10003 above	Lot of 8	$1,690		
10001	2 micron CMOS, 7.9 x 9.2 mm or smaller	Lot of 32	$9,810		
10002	Additional quantities of part #10001 above	Lot of 8	$2,440		
2. CMOS Analog 1.2 micron (priced per lot – includes packaging):					
10123	2.1 x 2.1 mm or smaller (Tiny)	Lot of 5	$850		
"	Additional quantities of Tiny parts	Lot of 5	$850		
10124	4.5 x 4.5 mm or smaller (Small)	Lot of 10	$3,360		
"	Additional quantities of Small parts	Lot of 10	$3,360		
10125	9.3 x 9.3 mm or smaller (Large)	Lot of 20	$12,840		
"	Additional quantities of Large parts	Lot of 20	$12,840		
3. 5X Reticle Runs (priced per sq mm – does not include packaging):					
10121	1.2 micron CMOS-5X (25 parts)	sq mm	$300		
10122	Additional quantities of 1.2u (Lot of 25)	sq mm	$230		
10119	0.8 micron CMOS-5X (25 parts)	sq mm	$390		
10120	Additional quantities of 0.8u (Lot of 25)	sq mm	$300		
10117	HGaAs3-5X (20 parts)	sq mm	$470		
10118	Additional quantities of HGaAs3 (Lot of 20)	sq mm	$360		
4. PACKAGING FOR 1.2 and 0.8 CIRCUITS:					
DIP28	28-pin DIP package	each	$18		
DIP40	40-pin DIP package	each	$18		
PGA65	65-pin PGA package	each	$33		
PGA84	84-pin PGA package	each	$33		
PGA108	108-PGA package	each	$33		
PGA132	132-PGA package	each	$33		

* Items marked with asterisks have not yet been assigned part numbers. All part numbers are subject to change.

Order form continued on next page

APPLICATION FOR ACCESS TO ARPA / NSF SILICON BROKERAGE SERVICE (MOSIS) TO SUPPORT EDUCATION

The National Science Foundation (NSF) and the Advanced Research Projects Agency (ARPA) are providing access to the ARPA/NSF Silicon Brokerage Service (MOSIS) to qualified universities for educational purposes. NSF sponsorship will be provided to U. S. universities and colleges, allowing them to use the MOSIS service for fabrication of integrated circuits designed by students enrolled in VLSI courses.

BACKGROUND

As part of ARPA's research in the VLSI area, they have developed a capability called MOSIS for fast turnaround fabrication of small quantities of custom VLSI chips. MOSIS is a brokerage service which aggregates the needs of a large design community and represents them to the U.S. semiconductor industry through a single interface.

Designs are submitted to MOSIS in digital form over electronic mail using standard design rules and standard artwork formats CIF or UU-Encoded GDS. The integrated circuits are fabricated at selected foundries, packaged and sent to the designer within a few weeks of submission to MOSIS.

The MOSIS service is located at the Information Sciences Institute of the University of Southern California (USC/ISI) located in Marina del Rey, California.

TERMS AND CONDITIONS

1. Access to the service will be on a controlled basis with use limited to those institutions meeting the requirements jointly established by NSF and ARPA. To qualify for funding under this program, universities must:

   a. Have adequate computer-aided design software to produce designs, simulate performance and generate either CIF or UU-Encoded GDS.

   b. Have the capability to transmit designs in either CIF or UU-Encoded GDS format to MOSIS over a computer network such as the Internet or CSNet. No physical media, e.g., magnetic tapes, floppy disks, etc., will be accepted.

   c. Have the capability and instrumentation to test the completed designs.

2. The university professor must provide a brief substantive report to MOSIS for each fabricated project. This report is to be submitted within three months after receipt of the packaged chips from MOSIS and must contain at least the following information:

   a. Number of packaged chips received;

b. Number tested for functionality;

c. Number of chips that were functional;

d. Comments on design errors, processing errors and errors of unknown source.

3. Universities will be required to comply with all operating rules governing the use of MOSIS.

4. NSF and ARPA reserve the right to limit use by individuals and institutions.

5. Neither NSF, ARPA or USC/ISI assume responsibility or liability for the units produced or the time required to produce them.

6. MOSIS will fabricate designs exactly as submitted. MOSIS will check that the layout file syntax is correct but will not validate designs.

7. The period of support will expire on September 30, 1993.

8. Universities specifically agree that they shall not disclose any material which may be considered proprietary or confidential material of USC/ISI or of any vendors to any third parties. Proprietary material shall include, but shall not be limited to, proprietary vendor information such as yield and parametric data, whether it was provided to customers or extracted by them.

PROPOSAL PREPARATION INSTRUCTIONS

Universities interested in obtaining educational use of the MOSIS Service are to fill out the attached MOSIS Service Application. The following must be attached to each application:

1. A narrative describing the program for which fabrication is desired. This is normally a description of a sequence of VLSI courses and their content.

2. Names and backgrounds of key personnel, including a point of contact, e.g., MOSIS liaison, at the University. The point of contact should be faculty or senior staff member.

Applications are to be signed by the department chairman and the professor who will act as MOSIS liaison. The original application is to be sent to the National Science Foundation and a copy is to be sent to the MOSIS Service at the following addresses:

NATIONAL SCIENCE FOUNDATION
SYSTEMS PROTOTYPING & FABRICATION
MIPS/ROOM 414
1800 "G" STREET NW
WASHINGTON, D.C. 20550

THE MOSIS SERVICE
CLASS APPLICATIONS
USC INFORMATION SCIENCES INSTITUTE
4676 ADMIRALTY WAY
MARINA DEL REY, CA 90292-6695

PROPOSAL EVALUATION CRITERIA

Each proposal will be evaluated based on a variety of factors, including:

1. Availability of adequate electronic communication access;
2. Adequacy and accessibility of CAD tools;
3. Capabilities and facilities for testing the completed chips (including appropriate schedule to adequately test the chips);
4. Qualification of the personnel involved;
5. Quality of VLSI education program and its contribution to the national VLSI education needs.

If your application is approved by NSF, you will be notified that a MOSIS account has been set up. Separate MOSIS accounts will be set up for introductory and advanced classes (see "Amount of Award" section).

ENROLLMENT CONFIRMATION FORMS

After your application is approved and an account has been established, you will be required to submit an Enrollment Confirmation Form at the beginning of each semester or quarter in which you are teaching classes that require fabrication. These forms identify the classes to be taught and list the actual number of students enrolled in each class. Enrollment Confirmation Forms are to be submitted within thirty days of the first day of classes. A blank form is attached; please make copies for your future use.

When your MOSIS account is initially set up, it will have a budget of zero. Funds are allocated to your account based on information in the Enrollment Confirmation Form.

AMOUNT OF AWARD

Budgets are allocated based on enrollment figures and the amount of available funds. The budget period begins upon approval of the Enrollment Confirmation Form and continues until September 30 of each year. At that time, all class budgets will be reset to zero. This is true regardless of when funds were added to your account.

Separate MOSIS accounts will be set up for introductory and advanced classes. An introductory class requires no other VLSI course as a prerequisite. An advanced class requires at least one VLSI course as a prerequisite. The current funding formulas are:

1. INTRODUCTORY CLASS: NSF is providing funds to cover fabrication of one (two micron) CMOS TinyChip for every two students. For example, in FY89/90 the cost of a two micron TinyChip was $450. The budget for a class with 20 students would be [(20 * $450) / 2] = $4,500. A two micron TinyChip has a total surface area of 2.22 mm x 2.25 mm edge-to-edge.

2. ADVANCED CLASS: Funds budgeted for advanced classes may not be used to support research or thesis projects unless those projects are a direct and integral part of the course (justification must be submitted with MOSIS Application and Enrollment Confirmation Forms).

BUDGET = I + GN + Q + MC

I = $5,000 Institutional grant from NSF (once per year per institution)

G = Grant per registered student (same as for beginning classes)

N = Number of registered students in advanced course

Q = Contribution by institution toward fabrication (optional)

M = Up to $5,000 matching funds provided by NSF (M = Q)

C = A constant (currently 1.0)

Budgets for Introductory and Advanced classes will be allocated according to the formulas above; however, classes will not be restricted to fabricating TinyChips. Some professors may choose to have a class fabricate fewer, larger chips. This is acceptable; however, budgets will still be allocated according to the formulas noted above. Larger chips are considerably more expensive and will deplete the budget much more quickly than TinyChips.

ADDITIONAL INFORMATION

If an organization's need for fabrication exceeds the amount of award, services can be purchased directly from MOSIS. Universities are eligible for a 10% discount off the published commercial MOSIS price schedule.

You may contact Wayne Tanner at (310) 822-1511 or <TANNER@MOSIS.EDU> for copies of the MOSIS design rules, fabrication schedule and additional MOSIS documentation. You may contact Helen Thompson at (310) 822-1511 or <HELEN@MOSIS.EDU> for other information.

Description of new design methodologies which simplify VLSI system designs are contained in the text *Introduction to VLSI Systems* by Mead and Conway (Addison-Wesley, 1981); in *Principles of CMOS VLSI Design: A Systems Perspective* by Weste and Eshraghian (Addison-Wesley, 1985); and in *The Design and Analysis of VLSI Circuits* by Glasser and Dobberpuhl (Addison-Wesley, 1985). Mead and Conway's text applies to NMOS circuits only, but their systems approach to VLSI design applies to CMOS as well.

Attachments: MOSIS Service Application Form
Enrollment Confirmation Form

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MOSIS SERVICE APPLICATION FORM

New Account _____

Renewal _____

MOSIS Account ID (if renewal) : _____

University : _____

Department : _____

Mailing Address: _____

_____

_____

Applicant (MOSIS Liaison): _____

Phone Number: _____

Network Address: _____

School Year: Semester _____ Quarter _____

==========

Please list all courses for which you require fabrication:

COURSE*	COURSE NAME	I or A*

* Introductory or Advanced (Introductory classes have no VLSI prerequisite)

==========

I certify that the information on this application is accurate and I agree to comply with the terms and conditions governing this program.

_____	_____
MOSIS Liaison signature	Department Chairman signature
_____	_____
Mosis Liaison typed name	Department Chairman typed name
_____	_____
(date signed)	(date signed)

Attachments: Narrative describing VLSI program

Background and qualifications of key personnel

MOSIS ENROLLMENT CONFIRMATION FORM

UNIVERSITY: _____

DEPARTMENT: _____

ADDRESS: _____

_____

_____

APPLICANT (MOSIS LIAISON) : _____

PHONE: _____ NET ADDRESS: _____

DATE CLASSES BEGIN: _____ DATE CLASSES END: _____

TESTING & SIMULATION TOOLS: _____

INTRODUCTORY CLASSES (MOSIS ACCOUNT: _____)

1. Course Number _____ Instructor: _____

   Course Name _____ # Students: _____
2. Course Number _____ Instructor: _____

   Course Name _____ # Students: _____

ADVANCED CLASSES (MOSIS ACCOUNT: _____)

1. Course Number _____ Instructor: _____

   Course Name _____ # Students: _____
2. Course Number _____ Instructor: _____

   Course Name _____ # Students: _____

I certify that the information on this form is accurate and the student count for each class represents the actual number of registered students (not estimates). In addition, I agree that no project will be submitted to MOSIS for fabrication until it has been logic tested and simulated.

_____	_____
MOSIS Liaison signature	Department Chairman signature
_____	_____
MOSIS Liaison typed name	Department Chairman typed name
_____	_____
(date signed)	(date signed)

Enclosures: Course descriptions
Background and qualiifications of professors

MOSIS TECHNOLOGY SHEET

Key Parameters from Vendors' Wafer Acceptance Specifications							
rams	Type	VLSI Technology 2u	Orbit 2u Pwell	Orbit 2u Nwell	HP 1.2um	HP 0.8um	Units
Tox		400 ± 30	400 ± 30	400 ± 30	200 ± 15	160 ± 10	Ang
*KP	N	> 48	46 ± 4	46 ± 3	93.2 ± 8.2	52.5 ± 2.1	uA/V^2
	P	> 18	14 ± 2	15 ± 3	34.5 ± 3.3	16.6 ± 1.5	
Vto	N	0.75 ± 0.15	0.8 ± 0.2	0.75 ± 0.25	0.7 ± 0.1	0.7 ± 0.07	Volt
	P	-0.75 ± 0.15	-0.8 ± 0.2	-0.75 ± 0.25	-0.9 ± 0.1	-0.9 ± 0.09	
Gamma	N	< 0.8	1.0 ± 0.2	0.25 ± 0.1	0.58 ± 0.1	0.56 ± 0.03	V^0.5
	P	< 0.8	0..5 ± 0.1	0.55 ± 0.1	0.50 ± 0.1	1.14 ± 0.08	
CJO	N	< 0.25	0.33	0.1	0.32 ± 0.03	0.36 ± 0.02	fF/um^2
	P	< 0.3	0.23	0.27	0.52 ± 0.05	0.46 ± 0.06	

*KP = u_oCox

Drawn Feature Size	# of Gates Per Square MM	Speed (Flip Flop Toggle Rate)
2.0u	250	35MHz
1.2u	700	75MHz
0.8u	1500	120MHz
Averages given will vary with layout style.		

The table below lists various combinations of design rule sets, vendors and feature sizes that can be fabricated through MOSIS. Pick the Technology Name that corresponds to your project's vendor/design rule set (e.g., SCN20 or SCPE20) and circle it on your Project Submission Form or enter it in your E-mail template; this information must accompany your layout geometry. See the back of this page for more information on project submission and technology descriptions.

Vendor	Technology Name		
	Vendor Design Rules	**CMOSN Design Rules**	**MOSIS Design Rules**
2u VLSI Technology N-well	VTI_CMN20	NSCx20 (x = N, E)	SCx20 (x = N, E)
2u Orbit P-well	ORBIT_CP20	NSCx20 (x = P, E)	SCxE20 (x = P, E) SCx20 (x = P, E)
2u Orbit N-well	ORBIT_CN20	NSCx20 (x = N, E)	SCxA20 (x = N, E) SCxE20 (x = N, E)
1.2uHP N-well	HP_CMOS34 (HP_AMOSI)	NSCx12 (x = N,E)	SCx12 (x = N,E) (SCxLC12 (x = N,E))
0.8uHP N-well	HP_CMOS26B	NSCx10 (x = N,E)	SCx10 (x = N,E) SCx3M10 (x = N, E)
Vitesse	VITESSE_HGAAS3	—	—

MOSIS Packaging

MOSIS–Supplied Packages (CMOS)

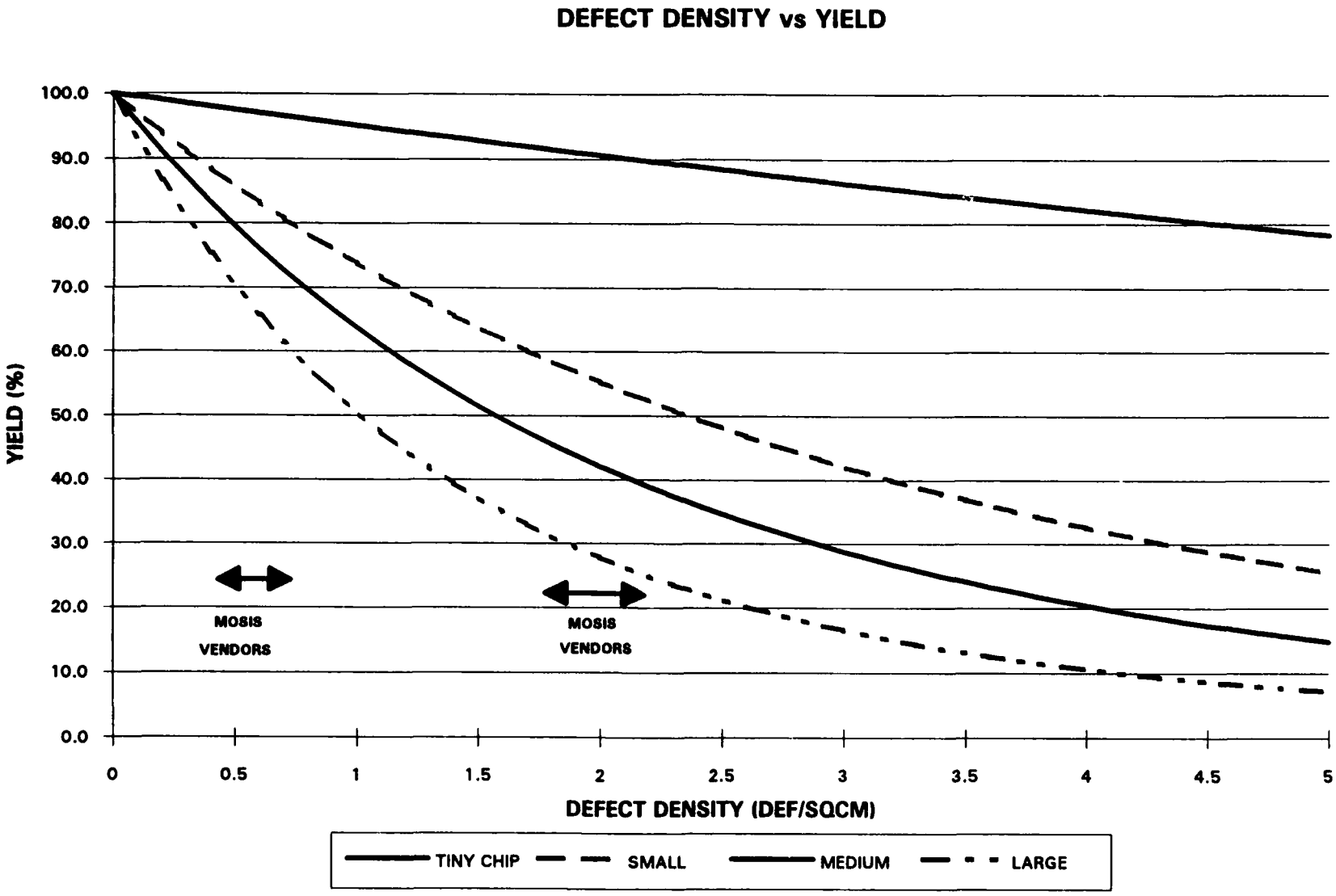
MOSIS offers the following standard commercial packages: 28 or 40 pin DIPs (Dual In–line Package) and 65, 84, 108, or 132 PGAs (Pin Grid Array). The package selected for a specific project depends on the number of pads in your design and on the size of the chip. MOSIS uses ceramic, cavity–up packages; the DIP packages are side–brazed. The following table summarizes the package and cavity sizes.

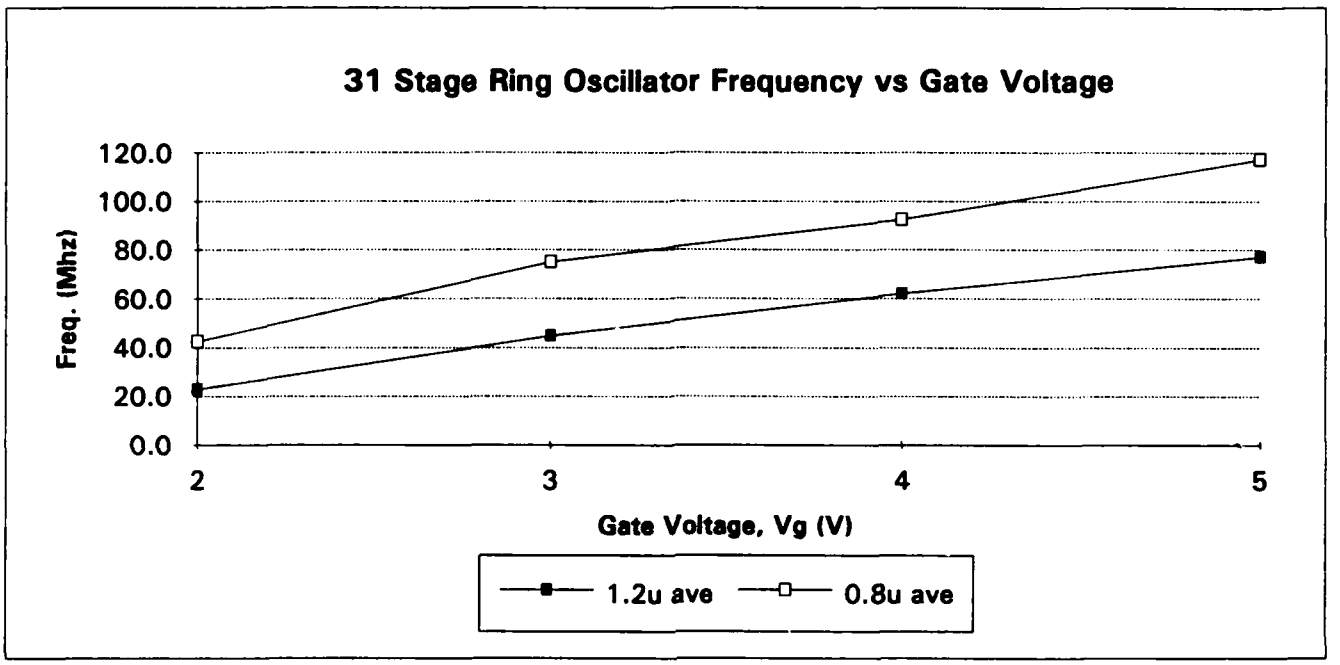
MOSIS Packages					
Pin Count	**Pkg Type**	**Cavity Size**	**Lead Resis.**	**Lead Induct.**	**Thermal Resist.**
28	0.6" DIP	.310 x .310"	350 mOHM	—	55 deg C/W
40	0.6" DIP	.310 x .310"	500 mOHM	—	45 deg C/W
65	1.0" PGA	.400 x 400"	600 mOHM	—	40 deg C/W
84	1.1" PGA	.350 x .350"	600 mOHM	7nH	40 deg C/W
84	1.1" PGA	.470 x 470"	600 mOHM	7nH	35 deg C/W
108	1.2" PGA	.350 x .350"	600 mOHM	11nH	35 deg C/W
108	1.2" PGA	.450 x .450"	600 mOHM	11nH	35 deg C/W
132	1.4" PGA	.350 x .350"	1500 mOHM	19nH	35 deg C/W
132	1.4" PGA	.450 x .450"	1500 mOHM	19nH	35 deg C/W

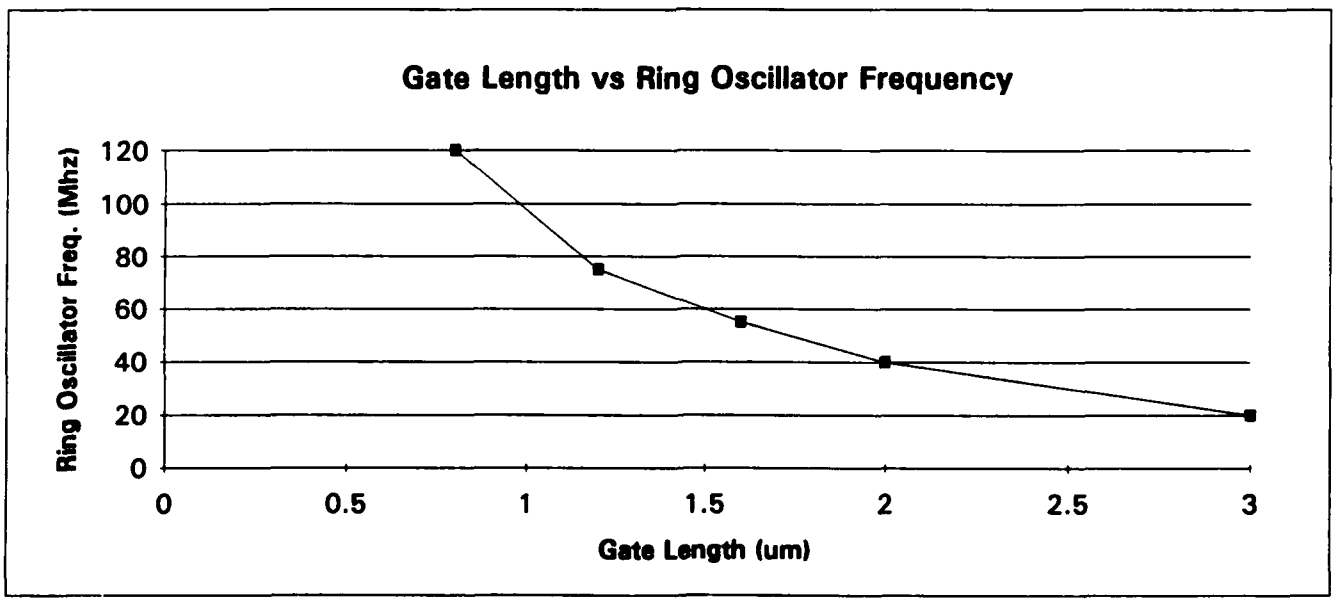
Note: Lead resistances and inductances are for signal lines; values for selected pins are lower. The junction to ambient (theta ja) thermal resistance is based upon a 10,000 square mil die, board mounted in still air. Thermal resistance varies with materials used, die size, process technology, air circulation and heat dissipation characteristics of the device.

User–Supplied Packages

If you would like to supply your own packages and lids, contact the MOSIS User Liaison or send MOSIS an Attention message; this MUST be done when you first submit your request for a Project–ID. At that time, MOSIS needs to know what type of package you wish to use (DIP, LCC, or PGA), the number of pins, and any other special features of the package. We regret that plastic packages are not available. When selecting the packages, allow for a cavity size that will accomodate the chip; 400 extra microns per side is usually adequate. However, if there is to be a downbond, allow an extra 100 microns on that side.


DEFECT DENSITY vs YIELD
100.0
90.0
80.0
70.0
60.0
50.0
40.0
30.0
20.0
10.0
0.0
YIELD (%)
MOSIS
VENDORS
MOSIS
VENDORS
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5
5
DEFECT DENSITY (DEF/SQCM)
TINY CHIP
SMALL
MEDIUM
LARGE


31 Stage Ring Oscillator Frequency vs Gate Voltage
Freq. (Mhz)
120.0
100.0
80.0
60.0
40.0
20.0
0.0
2
3
4
5
Gate Voltage, Vg (V)
1.2u ave
0.8u ave


Gate Length vs Ring Oscillator Frequency
Ring Oscillator Freq. (Mhz)
120
100
80
60
40
20
0
0
0.5
1
1.5
2
2.5
3
Gate Length (um)

MOSIS Process Monitor

The MOSIS Service

20 April 1989

1.0 INTRODUCTION

The MOSIS Process Monitor (PM) consists of an array of DC and AC parametric test structures and a small number of functional test devices for monitoring the fabrication of wafers for the MOSIS service. These tests are designed to monitor all of the parameters that are in the vendor process specification for each supported technology.

1.1 BASIC PARAMETRIC MONITORS AND PROBING ORGANIZATION

The test structures and tests described here are a basic parametric monitor set. This set is representative of the generic classes of structures required to monitor MOS wafer fabrication.

There are three classes of test devices: DC parametric, AC parametric, and Functional. Each class of test device has its own group of probe card pins. The DC parametric area consisting of a 2 x 10 pad group that is tested entirely by instrumentation within the Keithley parametric tester. The AC parametric area (capacitors) consists of a 2 x 2 pad group wired directly, through isolation relays, to the Hewlett Packard LCR meter which is interfaced to the Parametric Tester through the IEEE bus. Finally, the Functional Device Test area consists of a 2 x 10 pad group that is interfaced to a IMS Logic Master ST Plus functional test system which is also interfaced to the parametric tester through the IEEE 488 bus. This Functional Device Test area has been configured with preassigned function pins to make the functional tester programming and interface easier. The pin assignments for the functional pad group are included in section 1.4, Functional Test Structures.

In general, the set of test structures contained in this document are considered a library of test structures that can be used in PM's that suit particular requirements. In particular, MOSIS technologies that use full wafer masks have a rich set of structures in a full die "drop-in" PM, while in reticle (step and repeat) masking a minimal set of test structures are placed in a small test strip. In any case, the wafer selection process requires data on at least the following measurements:

TRANSISTOR CHARACTERISTICS
- Threshold
- Kp
- Gamma
- Delta Length, Delta Width
- Saturation current
- Punch through breakdown
- Junction breakdown
- Gate Oxide Thickness

SHEET RESISTANCE
- Resistance
- Line Width

CONTACT RESISTANCE
- Resistance
- Voltage Sum

RING OSCILLATOR
- Frequency

CAPACITORS for gate oxide capacitance
- Oxide Thickness

In addition, when space permits (e.g. full wafer lithography fabrication), the following additional tests are included:

CAPACITORS for measurement of all interlayer capacitances (analysis only)
- Area Capacitance
- Fringe Capacitance
- Edge Wall Capacitance

FIELD OXIDE TRANSISTORS
- Threshold

INVERTERS
- Vhigh
- Vlow
- Inverter Threshold (Vinv)
- Gain at Inverter Threshold

STEP COVERAGE
- Comb Isolation
- Serpentine Continuity

PATTERN GENERATOR
- Yield

1.2 DC PARAMETRIC TEST STRUCTURES

1.2.1 CONTACT RESISTANCE BRIDGES

The contact resistance bridges are Kelvin connected contact resistors with a single (nominal design rule) contact between two connected layers on the chip. They are specified as contacts between Metal1 (or Metal2) and some other layer. Metal1 (or Metal2 in the case of vias) is run in a "dog-leg" (bent 90 degrees in the center) bar of 15.0um width with a minimum contact (or via) placed center of the right angle jog. The connected layer is constructed with an identical structure rotated 180 degrees with the corner overlapping the metal. The width of this layer is also 15.0um. The ends of the four bars are each connected to separate probe pads.

1.2.1.1 TESTING

Testing is performed by passing constant current through the contact between the two layers and measuring the resulting voltage. The constant current source is attached to two opposite arms (of different layer type) of the bridge and the resulting voltage is measured between the remaining arms. With the current source at zero, the thermal voltage in the test structure is measured and later subtracted from the measured voltage. Current is passed in two directions and the measured voltages are summed (preserving the sign) to determine if the contact is partially rectifying. Usually, these tests are performed at two levels of current to assess the linearity of the resistance.

The resistance measured with the current in the positive direction is reported at both current levels. Voltage sums are reported for both current levels.

Resistance: $R = VMEASURE / IFORCE$

Voltage Sum: $VSUM = V(+IFORCE) + V(-IFORCE)$

IFORCE = 1.0 mA, for cuts
10.0 mA, for vias

1.2.2 SPLIT BRIDGES (Electrical Line Width and Sheet Resistance)

Sheet resistance and electrical line width are measured using a test structure called a Split Bridge. The Split Bridge consists of a Van der Pauw crossed bridge for sheet resistance measurement, a Kelvin line width measurement section, and a split wire section. The Van der Pauw section is a classic four arm structure, that has been used in the industry for many years, with arm widths of 25.0 um . The tap distances on the wire width section and the split wire section are the same and are determined by the technology design rule wire pitch. The unique feature of the Split Bridge is that the electrical wire width measurement structure is augmented by the split wire structure that enables measurement of the wire pitch. Measurement of the pitch is a valuable tool for detecting structural and/or instrumentation problems in the measurement process. The wire width section has a width equal to 2 * (min. wire width) + (min. wire spacing). The Split Bridges occupy four pad pairs and are constructed in every conducting layer in a technology.

In testing wafers fabricated using reticles and step and repeat lithography the split bridges are modified to save area in the test structure. Significant area savings are obtained by eliminating the split section and retaining only the sheet resistance and line width sections.

1.2.2.1 TESTING

Testing consists of three parts taken in the order described herein. The Van der Pauw test is performed first because the sheet resistance obtained from this portion of the test is used in subsequent tests.

The Van der Pauw measurement is done by passing constant current through two adjacent arms of the crossed bridge and measuring voltage on diagonal pairs of arms. The measurement is repeated with the pairs of arms for current force and for voltage sense rotated 90 degrees on the crossed bridge. The two voltage readings are averaged to remove any possible asymmetry in the bridge.

Wire width and split wire measurements are taken by passing constant current through the entire length of the structure and measuring the voltage between the taps on the wire and the split wire.

Sheet resistance is computed from:

RS = (pi/ln 2) * (AVMEASURE / IFORCE) Ohms/Sq.

where AVMEASURE = (VMEASURE1 + VMEASURE2) / 2,
pi = 3.1415927
ln () is the natural log.

IFORCE = 75 mA for Metal2
40 mA for Metal1
1.0 mA for Active and Poly
10.0 uA for Well

The line width is computed from:

W = (RS * L) / (VB / IFORCE) um

where IFORCE = test current
L = designed wire bridge tap spacing (120 um)
VB = measured wire bridge tap voltage

IFORCE = 40 mA for metal2
15 mA for metal1
0.1 mA for active area and poly
1.0 uA for well

Width Error is computed as follows:

W_error = W - W_drawn,

where W_drawn is as indicated in the text above.

Wire pitch is computed from:

P = RS*L*IFORCE*(2*VS - VB)/(2*VB*VS) um

where IFORCE = test current (same as the wire current)
VS = measured split bridge tap voltage
VB = measured wire bridge tap voltage

The above three computations are performed in the report generator software, which can also report width error from drawn and pitch error from design rule. In general there will be very little pitch error if the test is successful. The report generator will calculate deviation from as drawn wire width and pitch error. Pitch error will be used as part of the outlier filter process. A significant deviation of pitch from design value usually indicate measurement error or faulty test bridge, due to incomplete etch or topological defect.

1.2.3 ALIGNMENT BRIDGES

The purpose of the Alignment Bridges is to electrically measure the X and Y misalignment between contacts (cuts and vias) and the connected layers and between the two layers. Bridges are fabricated for Metal1 to Poly, Cut to Poly, Metal1 to Active, Cut to Active, Metal2 to Metal1, and Via to Metal1 alignment. From these measurements it is possible to derive other misalignments such as Poly to Active.

Alignment bridges consist of a rectangular traverse of the lower (contacted) layer with a wire of 15 um width such that the opening is (5.0 * min. layer width) um wide by (60.0 + min. wire width) um long. Taps (in the contacted layer) are placed at the center of the narrow ends and connected to two pads. A tap in the contacted layer is placed at the center of one long arm and connected to a pad (which is connected to the + voltage sense). The remaining long span has a contact (CUT or VIA, which is connected to the - voltage sense) placed in its center which may take two different forms.

A minimum geometry contact is used in the alignment of contact to layer test. Layer to layer alignment tests use an elongated contact with minimum width and a length of (2.0 * min. contact size + min. contacting layer width) um oriented with the long dimension of the contact parallel with and centered within the long layer span. In the case of the layer to layer alignment test a minimum width of the upper layer overlaps the elongated contact (and extends to the edge of the lower layer) at its center.

Two structures oriented orthogonally with each other form an alignment test. The orthogonal pair are not necessarily located in the same test block on the process monitor.

1.2.3.1 TESTING

Testing consists of passing constant current through the current force taps and measuring the differential voltage at the voltage sense taps. The magnitude of the current force is 0.2 mA for poly and active layers and 200 mA for the metal layers. By connecting the + current force to the +X or +Y end of the bridge misalignment voltages will bear the sign of the direction of misalignment.

The alignment error in microns is a computed parameter which requires data from the Split Bridges. The misalignment is computed from:

MA = (2*VM*FW)/(IF*RS) um

where RS = sheet resistance of the lower layer,
FW = fabricated electrical width = 15.0um + W_error (um)
IF = force current
VM = measured alignment voltage

1.2.4 LATCH-UP TEST STRUCTURE

The Latch-up Test Structure consists of a well plus N & P junctions and well plugs. The junctions are placed such that they are the minimum design rule distance from the well boundary. These structures are used to measure the betas of the parasitic bipolar transistors that are present in bulk CMOS. They occupy two pad pairs in the probe block.

1.2.4.1 TESTING

The NPN and PNP transistors are tested to obtain the forward and reverse beta characteristics of the devices. Forward beta is measured by using the active area junction as the emitter of the transistor and the well (or substrate) as the base. The lateral transistor will use the well as the collector. Reverse beta is measured by exchanging emitter and collector. The test procedure makes use of the parametric tester provided measurement code for bipolar devices. Beta is measured at 100 uA emitter current and 5.0 V collector voltage.

1.2.5 STEP COVERAGE TEST STRUCTURE

The Step Coverage Test is a structure constructed to monitor the metal step coverage. The structure is intended to be used to detect major process failures. In general there are not likely to be many failures due to poor metal step coverage on a structure of such small area.

The Metal1 geometry consists of a serpentine metal run between interdigitated fingers of metal running over oxide steps of polysilicon and active area at minimum design rule width and spacing. Metal2 step coverage is designed as above with the addition of minimum width and pitch metal1 running parallel to the poly and active.

The size of the step coverage test structure is determined by a bounding box specified at compile time. The metal1 and metal2 portions of the structure each occupy half of the available space on double metal runs.

1.2.5.1 TESTING

Testing the step coverage structure involves measuring the serpentine structure for continuity and measuring the interdigitated structures for electrical shorts.

The continuity test consists of current forced (IFORCE = 10.0 mA) through the serpentine with a voltage measurement to calculate a resistance. Note that an open circuit in the serpentine is easily detected by setting a voltage compliance limit on IFORCE and observing if the voltage limit is reached. Electrical shorts in the interdigitated structures are detected by applying a voltage (VFORCE = 5.0 V) between the serpentine and the comb and measuring the resulting current.

The parametric tester reports the voltage for the continuity test and the current for the short test. The report generator will evaluate the results of the test with a go - nogo boolean to indicate the presence or absence of shorts between interdigitated structures and the serpentine wire plus calculated wire resistance values of the serpentine wire.

1.2.6 THIN OXIDE TRANSISTORS

The test transistors are organized in several groups generally along the lines of variable Length, fixed Width; fixed Length, variable Width; and others. The transistor channel geometries listed below are generated in both N channel and P channel.

Test Transistor Sizes

L/W	@1.6um	@2.0um	@3.0um	
common				
Lmin-x/6(Wmin)	1.4/14.4	1.8/18.0	2.5/27.0	
Lmin/Wmin	1.6/2.4	2.0/3.0	3.0/4.5	#
Lmin/2(Wmin)	1.6/4.8	2.0/6.0	3.0/9.0	#
Lmin/6(Wmin)	1.6/14.4	2.0/18.0	3.0/27.0	#
Lmin/10(Wmin)	1.6/24.0	2.0/30.0	3.0/45.0	
Lmin/20(Wmin)	1.6/48.0	2.0/60.0	3.0/90.0	
Lmin/40(Wmin)	1.6/96.0	2.0/120.0	3.0/180.0	#
Lmin+x/6(Wmin)	1.8/14.4	2.2/18.0	3.5/27.0	
(3/2)Lmin/6(Wmin)	2.4/14.4	3.0/18.0	4.5/27.0	
(5/2)Lmin/6(Wmin)	4.0/14.4	5.0/18.0	7.5/27.0	
8(Lmin)/(Wmin)	12.8/2.4	16.0/3.0	24.0/4.5	
3(Lmin)/2(Wmin)	4.8/4.8	6.0/6.0	9.0/9.0	#
3(Lmin)/6(Wmin)	4.8/14.4	6.0/18.0	9.0/27.0	#
9(Lmin)/6(Wmin)	14.4/14.4	18.0/18.0	27.0/27.0	#
(25/2)Lmin/6(Wmin)	16.0/14.4	25.0/18.0	37.5/27.0	
Note: x = 0.2um @ 1.6, 2.0 and 0.5um @ 3.0				
isolated				
fixed size	50.0/50.0	50.0/50.0	50.0/50.0	
edgeless				
Lmin/40(Wmin)	1.6/96.0	2.0/120.0	3.0/180.0	

These sizes are intended for use in full characterization of the transistor process targets and for extraction of device model parameters. Transistor sizes marked with a # are the minimum set of transistors necessary for run acceptance or test strip purposes. In addition, the edgeless device is intended for evaluation of radiation hardness of the process.

1.2.6.1 TESTING

1.2.6.1.1 Tests performed on transistors are:

TRANSISTOR THRESHOLD VOLTAGE

Threshold voltages (Vth) are obtained form a conductivity curve which is a plot of drain current vs. gate voltage (Vg) for a drain voltage (Vd) that is much less than twice the Fermi potential (2 * phi). The absolute drain voltage is set at 50 mV. Threshold voltage is found by extrapolating the linear portion of the conductivity curve to Id = 0. The intersection of the extrapolated line is defined as the threshold voltage. Measurements must be made using at least three different body voltages (Vbs, 0.0, 2.5, and 5.0 volts).

PROCESS GAIN FACTOR

The slope of the conduction curve obtained in the threshold voltage measurement process is used to calculate the process gain factor (K') The slope (S) of the conduction curve is 2 * K * Vd. Therefore,

$$K = S / 2 * Vd.$$

Since K = K' * (W / L), then the process gain factor is calculated from K' = (S/2*Vd)*(L/W).

(Note: W and L must be corrected for as-fabricated W and L,
where W = W_drawn - DW, and L = L_drawn - DL.
W_drawn and L_drawn are measured in
EFFECTIVE CHANNEL WIDTH/LENGTH section.)

BODY EFFECT

The change in voltage threshold due to source to substrate (body) reverse bias is obtained from measurements of voltage threshold at different body reverse biases. Threshold voltages are measured at three different body voltages (0.0V, 2.5V, 5.0V; negative relative to source for N channel devices and positive relative to source for the P channel devices). Threshold voltages are measured in the manner described above.

SATURATION CURRENT

Saturation current is measured by connecting the gate to the drain (body connected to source) and applying Vgs=Vds= 5.0 volts and measuring current (Idss). The test transistor upon which this measurement is taken is: Lmin / 6(Wmin).

PUNCH THROUGH VOLTAGE

This test is performed only on short channel devices. The gate is connected to the source (body connected to source) and the drain is connected to a constant current supply. Punch through voltage (Vpt) is the resulting Vds. The test transistor is Lmin / 6(Wmin)

1.2.6.1.2 Tests performed on selected transistors include:

TRANSISTOR I/V CURVES

A selected set of tranisistors will be used to collect I/V curves for SPICE Model Parameters. Drain current (Ids) measurements will be made at various drain-source voltages (Vds), gate-source voltages (Vgs) and bulk-source voltages (Vbs). The specific set of transistor geometries and sets of bias voltages will be determined by the requirements of the parameter extractor. Provisions should be made to enter the temperature of the vacuum chuck at the time of the test either by manual entry or by automatic monitoring device.

ACTIVE AREA JUNCTION LEAKAGE

Junction leakage current is measured at a junction potential 5.0 V. Source/drain junction to well leakage is measured with the well connected to the bulk. Junction leakage will be measured on the drain of the 50/50 transistor structure with the gate and source floating.

ACTIVE AREA JUNCTION BREAKDOWN

Junction breakdown is measured by applying a reverse bias current of 1.0uA (positive for N junctions and negative for P junctions) and measuring the resulting junction voltage. Source/drain junction to well breakdown is measured with the well connected to the bulk. Measurements are made on the 50/50 transitor structure using the drain junction with the source and gate floating.

WELL JUNCTION BREAKDOWN

Well junction breakdown is measured by applying a reverse bias current of 1.0uA (positive for N junctions and negative for P junctions) and measuring the resulting junction voltage. Well to bulk junction breakdown will be measured on the the 50/50 transistor structure with the gate, drain and source connected to the well, and using the wafer chuck as the connection to the bulk. Since the well junction breakdown voltage tends to be large, it is possible that the parametric tester maximum current force compliance limit will be exceeded. In order to reduce the possibility of labeling a well junction as faulty (due to open connections to it) a test for rectifying junction must be performed before testing the

well junction breakdown. Then if the parametric tester maximum compliance limit is exceeded the test report can at least indicate that the breakdown voltage exceeds this limit.

DRAIN/SOURCE LEAKAGE

Drain/source leakage (Ids0) is measured with the gate connected to the source (body connected to source) and Vds= 5.0 volts. The transistor with length = Lmin and width = 40(Wmin) will be used for the leakage measurement. Measurements are made with gate and bulk connected to ground and a picoammeter connected between source and ground.

SUBTHRESHOLD CHARACTERISTICS

Subthreshold drain current is measured at Vds = 5.0V (body connected to source) and at Vgs ten equally spaced voltages between 0.0 and Vth. These measurements are performed only on the Lmin/40Wmin transistor. Measurements are made with bulk connected to ground and a picoammeter connected between source and ground. The subthreshold slope (in Decades/Volt) and correlation coefficient is calculated using linear regression.

EFFECTIVE CHANNEL WIDTH/LENGTH

Effective channel width and length are measured by extrapolation of the channel conductance of the as fabricated and the as drawn transistors. A value of the effective channel length and width is obtained by adding the delta length and delta width values to the drawn length and width. The transistors required for the delta_L measurement are: 25/2(Lmin)/6(Wmin) and 5/2(Lmin)/6(Wmin). The transistors required for tne delta_W measurement are: 8(Lmin)/10(Wmin) and 8(Lmin)/2(Wmin).

Delta Channel Length: DL = (L1*S1 - L2*S2) / (S1 -S2),

for transistors with: W1 = W2

Delta Channel Width: DW = (W1*S2 - W2*S1) / (S2-S1),

for transistors with: L1 = L2

where:
S1 = linear region slope of the larger device
S2 = linear region slope of the smaller device
L1 = drawn device length, larger device
L2 = drawn device length, smaller device
W1 = drawn device width , larger device
W2 = drawn device width, smaller device

Note:
L_effective = L_drawn - DL
W_effective = W_drawn - DW

1.2.7 THICK (FIELD) OXIDE TRANSISTORS

Thick oxide transistors consist of minimum active - to - active regions with the gap between them covered by metal1, metal2 or poly. In addition, a thick oxide transistor may be constructed with P-well (for P-well runs) to P+ regions at minimum spacing, covered by metal1, metal2, or poly. In this test device the P-well is the source.

1.2.7.1 TESTING

The threshold of the thick oxide devices are measured by a single point method. The drain is connected to the overlapping gate and a constant current source at iforce = 1.0uA is connected to the drain. The resulting voltage is measured and reported as the threshold.

1.2.8 VARIABLE RATIO INVERTERS

Inverters constructed with minimum channel length P and N channel transistors are contained in a group with common Vdd, Ground and inputs, separate outputs, and with ratios of 1.0, 1.5, 2.0. Channel lengths are Lmin and N channel widths are set to 2(Wmin).

1.2.8.1 TESTING

Each inverter is tested with Vdd set at the nominal operating voltage for the technology (e. g., Vdd=5.0 V. for 2.0 um CMOS). The output voltage is measured with the input connected to Vdd and Ground. The input is connected to the output and the resulting stable voltage is identified as the inverter threshold (Vinv). Finally the gain of the inverter is measured at an input voltage of Vinv.

1.3 AC PARAMETRIC TEST STRUCTURES

At the present the only AC parameters that will be monitored are the interlayer capacitances. At some later time the transistor small signal characteristics may be monitored.

The capacitor array consists of area capacitors (small perimeter), fringe capacitors (large perimeter), edge (net - net) capacitors, and crossover capacitors. In all cases, the capacitance measurements require further data reduction to render the desired information (e.g., extraction of the area component and the fringe component of capacitance). This data reduction is done in the report generator.

Topologically, all capacitors are designed to fit into the 2 x 10 pad block height of 240 um. The lengths of the capacitor structures are varied to obtain the desired capacitance, but are currently fixed at 300um. A full four point electrical structure is maintained to maximize the accuracy that is available from a general purpose LCR meter.

Capacitors that have one electrode connected to the well (either P-well or N-well) will have a substrate to well strap to assure that the stray capacitance can be compensated by one of the two calibration capacitors.

1.3.0.1 NULL CAPACITOR (Calibration Capacitor)

Two four pad "null" capacitors are provided on the dropin to measure and store the stray capacitance associated with the test fixture for deduction from subsequent measurements. These two calibration capacitors are configured topologically to occupy two adjacent 2 x 2 slots in the capacitor array section of the PCM die. One calibration capacitor is floating so it can be used to calibrate out stray capacitances involved in measuring capacitors that do not have one electrode connected to the substrate (e.g., a metal1 to metal1 edge capacitor). The other calibration capacitor has one electrode connected to the substrate to calibrate out stray capacitances that are seen when measuring capacitors that use the substrate as one electrode (e.g., metal2 to substrate).

1.3.1 AREA CAPACITORS

The area capacitors are designed with the top electrode dimensions set at 240 um high by 300 um wide. This provides at least 1.0 pF capacitance from the field oxide capacitors.

1.3.1.1 TESTING

Measurements are made with an AC test voltage of 100mV rms and a frequency of 1.0MHz. Other test requirements, as yet undefined, could require other values of test voltage and test frequency.

Basic thin oxide capacitor measurements for the purposes of determining the thickness of the gate oxide will use a bias potential of magnitude and sign that will cause heavy inversion of the oxide semiconductor interface. Since thin oxide capacitors are essentially large area transistors with drain and source connected together the bias voltage magnitude is determined by the process target operating voltage.

All other capacitors are tested at zero bias voltage.

Geometrical parameters are:

Area: Aa = H * L um**2

Perimeter: Pa = (2 * H) + (2 * L) um

where H = top electrode height
L = top electrode length

Thin oxide capacitor measurements are used in the computation of the oxide thickness with the following equation:

Tox = (Aa * 3.3468E-11) / Cam

where Cam = measured capacitance of the area capacitor

Interlayer insulator capacitor measurements can be used to calculate the thickness of the insulator by using the above equation if the interlayer insulator is silicon dioxide. If the layer insulation is some other material (e.g., silicon nitride or combination of both) the more general form of the equation must be used:

Tins = E * E0 * (Aa / Cam)

where E = effective dielectric constant of the insulator

and E0 = permitivity of free space = 8.854e-12 Farad/m

1.3.2 FRINGE CAPACITORS

The fringe capacitors are comb structures with a comb width of 10 um and a comb spacing of 10um. The height is slightly smaller than 240 um, the maximum height permitted by the capacitor structures. Top electrode length is 300 um.

1.3.2.1 TESTING

Measurements are made with an AC test voltage of 100mV rms and a frequency of 1.0MHz. Other test requirements, as yet undefined, could require other values of test voltage and test frequency.

Capacitors with thin oxide between the layers must be measured at zero volts bias to obtain the gate overlap capacitance.

Junction capacitors are measured with a zero bias voltage.

Field oxide capacitors are measured with a voltage applied to cause strong accumulation. The magnitude of this voltage is determined by the technology (e. g., for 3.0 um CMOS the voltage is 10 volts).

Geometrical parameters are:

Area: Af = (NR * H * 10) + ((NR - 1) * 10 * 10) um**2

Perimeter: Pf = (H * 2) + (NR * 2 * 10) + ((NR - 1) * 2 * H) um

where NR = INT(L / 20)
H = top electrode height
L = top electrode length

Computation of component capacitances (e.g., junction: CJSW and CJ) using the area capacitor measurements and the fringe capacitor measurements is done with the following equations:

Fringe capacitance:

$$Cf = ((Cam/Aa) - (Cfm/Af)) / ((Pa/Aa) - (Pf/Af)) \qquad pF/um$$

Area capacitance:

$$Ca = (Cam/Aa) - Cf*(Pa/Aa) \qquad pF/um^{**2}$$

where Cam = measured capacitance on the area capacitor
Cfm = measured capacitance on the fringe capacitor

1.3.3 EDGE (NET TO NET) CAPACITORS

Net to net capacitors are intended to directly measure the capacitance between parallel runs of wires in the same layer with minimun design rule spacing. These capacitors are interdigitated double combs (fish bone structures) with minimum wire width and spacing. This topology minimizes parasitic resistance in series with the capacitance being measured.

These capacitors are generated for only metal1, metal2 and polysilicon. There is an maximum integer number of comb structures computed to fit within a length of 300 um.

1.3.3.1 TESTING

Measurements are made with an AC test voltage of 100mV rms and a frequency of 1.0MHz. Other test requirements, as yet undefined, could require other values of test voltage and test frequency.

Capacitances are measured at zero bias voltage.

Geometrical parameters are:

Edge Length: $Le = 2*N*((H - 10) + (W * 2) + (S * 2))$

where S = min. design rule spacing
W = min. design rule width
N = INT(L / (2*W + 2*S))
H = top electrode height
L = top electrode length

Edge capacitance:

$$Ce = (Cem / Le) \qquad pF/um$$

where Cem = measured capacitance on the edge capacitor

1.3.4 CROSSOVER CAPACITORS

The crossover capacitance tests consist of crossings of Metal1, Metal2 and Metal1, Poly to measure the total capacitance per crossing. They consist of parallel runs of the lower layer crossed by orthogonal runs of the upper layer. The sizes and number of crossings are used to compute the "excess capacitance" per crossing that would be predicted from just the area capacitance contribution. The number of crossings is determined by the upper electrode length and the layer (the height is 240 um) and is generated by filling the available space with the maximum integer number of upper and lower layer runs that is allowed by

the space available.

1.3.4.1 TESTING

Measurements are made with an AC test voltage of 100mV rms and a frequency of 1.0MHz. Other test requirements, as yet undefined, could require other values of test voltage and test frequency.

Geometrical parameters are:

Number of crossings:

$Nc = Nx * Ny$

where
$Nx = INT(L / (W2 + S2))$
$Ny = INT((H + W1) / (W1 + S1))$
$S1$ = min. design rule spacing of top electrode
$W1$ = min. design rule width of top electrode
$S2$ = min. design rule spacing of bottom electrode
$W2$ = min. design rule width of bottom electrode
H = top electrode height
L = top electrode length

Crossover capacitance:

$Cc = (Ccm / Nc)$ pF/um

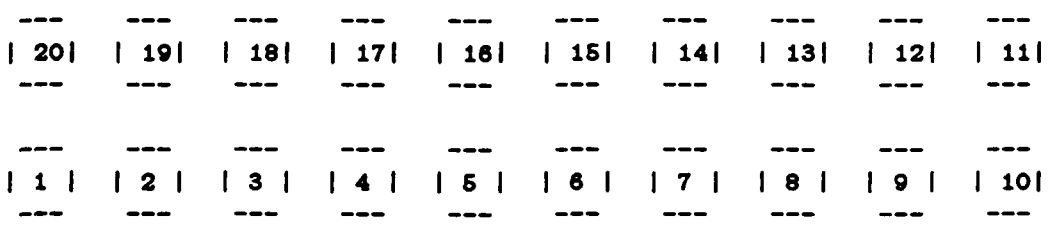
where Ccm = measured capacitance on the crossover capacitor

1.4 FUNCTIONAL TEST STRUCTURES

The functional test structures are intended to be used to evaluate the performance of the extracted model parameters and to act as an alarm for a low yield fabrication run if there are serious flaws in fabrication.

They will provide performance information on the standard cell circuits present on the run.

The parametric test area is configured so that the pin-out is standardized to minimize the complexity of the interface to test equipment. This pin-out is defined assuming the following pin numbering convention:



Assigned pin functions are defined as follows:

Pin #	Function
1	Clock
2	Input/Output
3	Input/Output
4	Input/Output
5	Input/Output
6	Input/Output

7	Input/Output
8	Input/Output
9	Input/Output
10	Ground
11	Input/Output and Ring Oscillator ENABLE
12	Input/Output
13	Input/Output
14	Input/Output
15	Input/Output
16	Input/Output
17	Input/Output
18	Input/Output
19	Ring Oscillator Output
20	Vdd

The Input/Output pins and the Clock are interfaced with the Test Pods that are connected with the functional tester. The drive lines of these Pods are tristatable and are parallelled with the Acquisition Pods to permit flexable utilization of the 16 functional I/O pins. Pin 11 is also connected to a small relay that can connect the Ring Oscillator ENABLE signal to this pin. The purpose of the relay is to reduce the stray capacitance associated with the ENABLE signal wire.

1.4.1 RING OSCILLATOR

The ring oscillator is a 31 stage string of inverters with a ratio of two. The inverter transistors have a N channel width of twice minimum and a channel length of minimum. The inverter ring is buffered with three stages of geometrically growing inverters such that it is capable of driving the interconnect capacitance to the frequency counter buffer. This buffer is a unity gain amplifier with 100 MHz bandwidth and a capability of driving a coaxial cable with a 50-Ohm termination.

1.4.1.1 TESTING

The parametric tester supplies power (Vdd and ground) to the device under test through the probe card interface board. A relay is activated to connect a parametric tester pin to the ring oscillator enable pin and a disable voltage (equal to Vdd) is applied to supress any multimode oscillation that may be present. The disable voltage is removed to start oscillation and a frequency measurement is taken.

The IEEE bus is used to command up to five measurements of frequency from the frequency counter. The parametric tester will compute the average of two consecutive frequency measurements in which the second reading is within 10% of the first. Up to five readings are taken until the above condition is achieved. If acceptable readings are not found then the structure is considered inoperative.

The parametric tester will report the average of two frequency measurements.

1.4.2 DYNAMIC SHIFT REGISTER

The dynamic shift register is a master - slave two phase clocked shift register that is eight bits wide and six words long. The two phase clock (with complements) is generated in the test structure. The functional tester need only provide data and a single phase clock that is true when data is stable.

1.4.2.1 TESTING

The shift register is supplied Vdd and Ground from the parametric tester and is clocked at 1.0 MHz by the functional tester to determine if it is functioning. The supply current is logged for future reference during data reduction.

If the Dynamic Shift Register is fully functional a value of 1.0 is logged and if it is not functional a value 0.0 is logged. No attempt is made to log the failure pattern.

1.4.3 PATTERN GENERATOR

The pattern generator is a 511 bit maximum length pseudorandom number generator constructed from CMOS3 Library standard cells (or equivalents). The cells used are:

XOR (2310)
D-FF with S/RESET (1480)
INVERTER PAIR (1100)
NON-INVERTING OUTPUT BUFFER (1510)

It is a modular shift register generator with 9 stages with feedback from the 9th stage modulo-2 added with the output of 6th, 4th, 3rd, 2nd and 1st stages and fed to the inputs of 7th, 5th, 4th, 3rd and 2nd stages, respectively. A logic diagram illustrating the setup is as follows: (see figure)

(Figure not available on-line)

1.4.3.1 TESTING

The pattern generator is clocked at 1 MHz and its output tested for the expected sequence of bits.

If the Pattern Generator is fully functional a value of 1 is logged and if it is not functional a value of 0 is logged. No attempt is made to log the failure pattern.

Appendix I - Test structure nomenclature IDs

Test structures on MOSIS generated process monitors have nomenclature identification. These IDs help locate a particular structure within the process monitor. The following lists the test structures titles and their corresponding ID.

Test Block Title	ID
Alignment bridge METAL1 to P_PLUS_ACTIVE in Y	A1
Alignment bridge CUT to N_PLUS_ACTIVE in X	A2
Alignment bridge CUT to N_PLUS_ACTIVE in Y	A3
Alignment bridge METAL1 to POLY_N_PLUS in X	A4
Alignment bridge METAL1 to POLY_N_PLUS in Y	A5
Alignment bridge CUT to POLY_P_PLUS in X	A6
Alignment bridge CUT to POLY_P_PLUS in Y	A7
Alignment bridge METAL2 to METAL1 in X	A8
Alignment bridge METAL2 to METAL1 in Y	A9
Alignment bridge VIA to METAL1 in X	A10
Alignment bridge VIA to METAL1 in Y	A11
Alignment bridge METAL1 to P_PLUS_ACTIVE in X	A12
Alignment bridge METAL1 to ELECTRODE in X	A20
Alignment bridge METAL1 to ELECTRODE in Y	A21
Alignment bridge CUT to ELECTRODE in X	A22
Alignment bridge CUT to ELECTRODE in Y	A23
Crossover Capacitor METAL2 to METAL1	C1
Crossover Capacitor METAL1 to POLY	C2
Edge Capacitor POLY to POLY	C3
Edge Capacitor METAL2 to METAL2	C4
Edge Capacitor METAL1 to METAL1	C5
Fringe Capacitor POLY to N_PLUS_ACTIVE	C6
Fringe Capacitor POLY to P_PLUS_ACTIVE	C7
Fringe Capacitor N_PLUS_ACTIVE to P_WELL	C8
Fringe Capacitor P_PLUS_ACTIVE to N_WELL	C9
Area Capacitor METAL2 to POLY	C10
Area Capacitor METAL1 to POLY	C11
Area Capacitor METAL2 to METAL1	C12
Area Capacitor METAL2 to N_PLUS_ACTIVE	C13
Area Capacitor METAL1 to N_PLUS_ACTIVE	C14
Area Capacitor METAL2 to N_WELL	C15
Area Capacitor METAL1 to N_WELL	C16
Area Capacitor POLY to N_WELL	C17
Area Capacitor N_PLUS_ACTIVE to P_WELL	C18
Area Capacitor P_PLUS_ACTIVE to N_WELL	C19
Area Capacitor POLY to N_PLUS_ACTIVE	C20
Area Capacitor POLY to P_PLUS_ACTIVE	C21
Calibration Capacitor with connected substrate	C22
Calibration Capacitor floating	C23
Area Capacitor ELECTRODE to POLY	C30
Area Capacitor METAL1 to ELECTRODE	C31
Area Capacitor METAL2 to ELECTRODE	C32

Dynamic Shift Register	F1
Pattern Generator	F2
Ring Oscillator	F3
XOR tree	F4
Ring Oscillator trio	F6
Ring Oscillator pair	F7
Test inverter(s)	I1
Poly (P+) bridge	K1
Poly (N+) bridge	K2
P+ Active bridge	K3
N+ Active bridge	K4
Metal bridge	K5
Second_metal bridge	K6
P-Well bridge	K7
N-Well bridge	K8
P+ Active to Metal contact	K9
Second Metal to First Metal contact	K10
Poly bridge	K11
Poly (P+) to Metal contact	K12
Poly (N+) to Metal contact	K13
N+ Active to Metal contact	K14
P-Well under Poly bridge	K15
N-Well under Poly bridge	K16
Electrode bridge	K20
Electrode to Metal contact	K21
Latchup Beta Transistors	L1
Step coverage METAL1 METAL2	S1
Step control METAL1 METAL2	S2
Step coverage METAL2	S3
Step control METAL2	S4
Step coverage METAL1	S5
Step control METAL1	S6
N_ENHANCEMENT common transistor(s)	T1
P_ENHANCEMENT common transistor(s)	T2
N_ACT field oxide transistors	T3
P_ACT field oxide transistors	T4
N_ENHANCEMENT isolated transistor(s)	T5
P_ENHANCEMENT isolated transistor(s)	T6
N_ENHANCEMENT closed transistor	T7
P_ENHANCEMENT closed transistor	T8

MOSIS Process Monitor

The MOSIS Service

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1.0 INTRODUCTION

The MOSIS Process Monitor (PM) consists of an array of DC and AC parametric test structures and a small number of functional test devices for monitoring the fabrication of wafers for the MOSIS service. These tests are designed to monitor all of the parameters that are in the vendor process specification for each supported technology.

1.1 BASIC PARAMETRIC MONITORS AND PROBING ORGANIZATION

The test structures and tests described here are a basic parametric monitor set. This set is representative of the generic classes of structures required to monitor MOS wafer fabrication.

There are three classes of test devices: DC parametric, AC parametric, and Functional. Each class of test device has its own group of probe card pins. The DC parametric area consisting of a 2 x 10 pad group that is tested entirely by instrumentation within the Keithley parametric tester. The AC parametric area (capacitors) consists of a 2 x 2 pad group wired directly, through isolation relays, to the Hewlett Packard LCR meter which is interfaced to the Parametric Tester through the IEEE bus. Finally, the Functional Device Test area consists of a 2 x 10 pad group that is interfaced to a IMS Logic Master ST Plus functional test system which is also interfaced to the parametric tester through the IEEE 488 bus. This Functional Device Test area has been configured with preassigned function pins to make the functional tester programming and interface easier. The pin assignments for the functional pad group are included in section 1.4, Functional Test Structures.

In general, the set of test structures contained in this document are considered a library of test structures that can be used in PM's that suit particular requirements. In particular, MOSIS technologies that use full wafer masks have a rich set of structures in a full die "drop-in" PM, while in reticle (step and repeat) masking a minimal set of test structures are placed in a small test strip. In any case, the wafer selection process requires data on at least the following measurements:

TRANSISTOR CHARACTERISTICS
- Threshold
- Kp
- Gamma
- Delta Length, Delta Width
- Saturation current
- Punch through breakdown
- Junction breakdown
- Gate Oxide Thickness

SHEET RESISTANCE
- Resistance
- Line Width

CONTACT RESISTANCE
- Resistance
- Voltage Sum

RING OSCILLATOR
- Frequency

CAPACITORS for gate oxide capacitance
- Oxide Thickness

In addition, when space permits (e.g. full wafer lithography fabrication), the following additional tests are included:

CAPACITORS for measurement of all interlayer capacitances (analysis only)
- Area Capacitance
- Fringe Capacitance
- Edge Wall Capacitance

FIELD OXIDE TRANSISTORS
- Threshold

INVERTERS
- Vhigh
- Vlow
- Inverter Threshold (Vinv)
- Gain at Inverter Threshold

STEP COVERAGE
- Comb Isolation
- Serpentine Continuity

PATTERN GENERATOR
- Yield

1.2 DC PARAMETRIC TEST STRUCTURES

1.2.1 CONTACT RESISTANCE BRIDGES

The contact resistance bridges are Kelvin connected contact resistors with a single (nominal design rule) contact between two connected layers on the chip. They are specified as contacts between Metal1 (or Metal2) and some other layer. Metal1 (or Metal2 in the case of vias) is run in a "dog-leg" (bent 90 degrees in the center) bar of 15.0um width with a minimum contact (or via) placed center of the right angle jog. The connected layer is constructed with an identical structure rotated 180 degrees with the corner overlapping the metal. The width of this layer is also 15.0um. The ends of the four bars are each connected to separate probe pads.

1.2.1.1 TESTING

Testing is performed by passing constant current through the contact between the two layers and measuring the resulting voltage. The constant current source is attached to two opposite arms (of different layer type) of the bridge and the resulting voltage is measured between the remaining arms. With the current source at zero, the thermal voltage in the test structure is measured and later subtracted from the measured voltage. Current is passed in two directions and the measured voltages are summed (preserving the sign) to determine if the contact is partially rectifying. Usually, these tests are performed at two levels of current to assess the linearity of the resistance.

The resistance measured with the current in the positive direction is reported at both current levels. Voltage sums are reported for both current levels.

Resistance: R = VMEASURE / IFORCE

Voltage Sum: VSUM = V(+IFORCE) + V(-IFORCE)

IFORCE = 1.0 mA, for cuts
10.0 mA, for vias

1.2.2 SPLIT BRIDGES (Electrical Line Width and Sheet Resistance)

Sheet resistance and electrical line width are measured using a test structure called a Split Bridge. The Split Bridge consists of a Van der Pauw crossed bridge for sheet resistance measurement, a Kelvin line width measurement section, and a split wire section. The Van der Pauw section is a classic four arm structure, that has been used in the industry for many years, with arm widths of 25.0 um . The tap distances on the wire width section and the split wire section are the same and are determined by the technology design rule wire pitch. The unique feature of the Split Bridge is that the electrical wire width measurement structure is augmented by the split wire structure that enables measurement of the wire pitch. Measurement of the pitch is a valuable tool for detecting structural and/or instrumentation problems in the measurement process. The wire width section has a width equal to 2 * (min. wire width) + (min. wire spacing). The Split Bridges occupy four pad pairs and are constructed in every conducting layer in a technology.

In testing wafers fabricated using reticles and step and repeat lithography the split bridges are modified to save area in the test structure. Significant area savings are obtained by eliminating the split section and retaining only the sheet resistance and line width sections.

1.2.2.1 TESTING

Testing consists of three parts taken in the order described herein. The Van der Pauw test is performed first because the sheet resistance obtained from this portion of the test is used in subsequent tests.

The Van der Pauw measurement is done by passing constant current through two adjacent arms of the crossed bridge and measuring voltage on diagonal pairs of arms. The measurement is repeated with the pairs of arms for current force and for voltage sense rotated 90 degrees on the crossed bridge. The two voltage readings are averaged to remove any possible asymmetry in the bridge.

Wire width and split wire measurements are taken by passing constant current through the entire length of the structure and measuring the voltage between the taps on the wire and the split wire.

Sheet resistance is computed from:

RS = (pi/ln 2) * (AVMEASURE / IFORCE) Ohms/Sq.

where AVMEASURE = (VMEASURE1 + VMEASURE2) / 2,
pi = 3.1415927
ln () is the natural log.

IFORCE = 75 mA for Metal2
40 mA for Metal1
1.0 mA for Active and Poly
10.0 uA for Well

The line width is computed from:

W = (RS * L) / (VB / IFORCE) um

where IFORCE = test current
L = designed wire bridge tap spacing (120 um)
VB = measured wire bridge tap voltage

IFORCE = 40 mA for metal2
15 mA for metal1
0.1 mA for active area and poly
1.0 uA for well

Width Error is computed as follows:

W_error = W - W_drawn,

where W_drawn is as indicated in the text above.

Wire pitch is computed from:

P = RS*L*IFORCE*(2*VS - VB)/(2*VB*VS) um

where IFORCE = test current (same as the wire current)
VS = measured split bridge tap voltage
VB = measured wire bridge tap voltage

The above three computations are performed in the report generator software, which can also report width error from drawn and pitch error from design rule. In general there will be very little pitch error if the test is successful. The report generator will calculate deviation from as drawn wire width and pitch error. Pitch error will be used as part of the outlier filter process. A significant deviation of pitch from design value usually indicate measurement error or faulty test bridge, due to incomplete etch or topological defect.

1.2.3 ALIGNMENT BRIDGES

The purpose of the Alignment Bridges is to electrically measure the X and Y misalignment between contacts (cuts and vias) and the connected layers and between the two layers. Bridges are fabricated for Metal1 to Poly, Cut to Poly, Metal1 to Active, Cut to Active, Metal2 to Metal1, and Via to Metal1 alignment. From these measurements it is possible to derive other misalignments such as Poly to Active.

Alignment bridges consist of a rectangular traverse of the lower (contacted) layer with a wire of 15 um width such that the opening is (5.0 * min. layer width) um wide by (60.0 + min. wire width) um long. Taps (in the contacted layer) are placed at the center of the narrow ends and connected to two pads. A tap in the contacted layer is placed at the center of one long arm and connected to a pad (which is connected to the + voltage sense). The remaining long span has a contact (CUT or VIA, which is connected to the - voltage sense) placed in its center which may take two different forms.

A minimum geometry contact is used in the alignment of contact to layer test. Layer to layer alignment tests use an elongated contact with minimum width and a length of (2.0 * min. contact size + min. contacting layer width) um oriented with the long dimension of the contact parallel with and centered within the long layer span. In the case of the layer to layer alignment test a minimum width of the upper layer overlaps the elongated contact (and extends to the edge of the lower layer) at its center.

Two structures oriented orthogonally with each other form an alignment test. The orthogonal pair are not necessarily located in the same test block on the process monitor.

1.2.3.1 TESTING

Testing consists of passing constant current through the current force taps and measuring the differential voltage at the voltage sense taps. The magnitude of the current force is 0.2 mA for poly and active layers and 200 mA for the metal layers. By connecting the + current force to the +X or +Y end of the bridge misalignment voltages will bear the sign of the direction of misalignment.

The alignment error in microns is a computed parameter which requires data from the Split Bridges. The misalignment is computed from:

MA = (2*VM*FW)/(IF*RS) um

where RS = sheet resistance of the lower layer,
FW = fabricated electrical width = 15.0um + W_error (um)
IF = force current
VM = measured alignment voltage

1.2.4 LATCH-UP TEST STRUCTURE

The Latch-up Test Structure consists of a well plus N & P junctions and well plugs. The junctions are placed such that they are the minimum design rule distance from the well boundary. These structures are used to measure the betas of the parasitic bipolar transistors that are present in bulk CMOS. They occupy two pad pairs in the probe block.

1.2.4.1 TESTING

The NPN and PNP transistors are tested to obtain the forward and reverse beta characteristics of the devices. Forward beta is measured by using the active area junction as the emitter of the transistor and the well (or substrate) as the base. The lateral transistor will use the well as the collector. Reverse beta is measured by exchanging emitter and collector. The test procedure makes use of the parametric tester provided measurement code for bipolar devices. Beta is measured at 100 uA emitter current and 5.0 V collector voltage.

1.2.5 STEP COVERAGE TEST STRUCTURE

The Step Coverage Test is a structure constructed to monitor the metal step coverage. The structure is intended to be used to detect major process failures. In general there are not likely to be many failures due to poor metal step coverage on a structure of such small area.

The Metal1 geometry consists of a serpentine metal run between interdigitated fingers of metal running over oxide steps of polysilicon and active area at minimum design rule width and spacing. Metal2 step coverage is designed as above with the addition of minimum width and pitch metal1 running parallel to the poly and active.

The size of the step coverage test structure is determined by a bounding box specified at compile time. The metal1 and metal2 portions of the structure each occupy half of the available space on double metal runs.

1.2.5.1 TESTING

Testing the step coverage structure involves measuring the serpentine structure for continuity and measuring the interdigitated structures for electrical shorts.

The continuity test consists of current forced (IFORCE = 10.0 mA) through the serpentine with a voltage measurement to calculate a resistance. Note that an open circuit in the serpentine is easily detected by setting a voltage compliance limit on IFORCE and observing if the voltage limit is reached. Electrical shorts in the interdigitated structures are detected by applying a voltage (VFORCE = 5.0 V) between the serpentine and the comb and measuring the resulting current.

The parametric tester reports the voltage for the continuity test and the current for the short test. The report generator will evaluate the results of the test with a go - nogo boolean to indicate the presence or absence of shorts between interdigitated structures and the serpentine wire plus calculated wire resistance values of the serpentine wire.

1.2.6 THIN OXIDE TRANSISTORS

The test transistors are organized in several groups generally along the lines of variable Length, fixed Width; fixed Length, variable Width; and others. The transistor channel geometries listed below are generated in both N channel and P channel.

Test Transistor Sizes

L/W	@1.6um	@2.0um	@3.0um	
common				
Lmin-x/6(Wmin)	1.4/14.4	1.8/18.0	2.5/27.0	
Lmin/Wmin	1.6/2.4	2.0/3.0	3.0/4.5	#
Lmin/2(Wmin)	1.6/4.8	2.0/6.0	3.0/9.0	#
Lmin/6(Wmin)	1.6/14.4	2.0/18.0	3.0/27.0	#
Lmin/10(Wmin)	1.6/24.0	2.0/30.0	3.0/45.0	
Lmin/20(Wmin)	1.6/48.0	2.0/60.0	3.0/90.0	
Lmin/40(Wmin)	1.6/96.0	2.0/120.0	3.0/180.0	#
Lmin+x/6(Wmin)	1.8/14.4	2.2/18.0	3.5/27.0	
(3/2)Lmin/6(Wmin)	2.4/14.4	3.0/18.0	4.5/27.0	
(5/2)Lmin/6(Wmin)	4.0/14.4	5.0/18.0	7.5/27.0	
8(Lmin)/(Wmin)	12.8/2.4	16.0/3.0	24.0/4.5	
3(Lmin)/2(Wmin)	4.8/4.8	6.0/6.0	9.0/9.0	#
3(Lmin)/6(Wmin)	4.8/14.4	6.0/18.0	9.0/27.0	#
9(Lmin)/6(Wmin)	14.4/14.4	18.0/18.0	27.0/27.0	#
(25/2)Lmin/6(Wmin)	16.0/14.4	25.0/18.0	37.5/27.0	
Note: x = 0.2um @ 1.6, 2.0 and 0.5um @ 3.0				
isolated				
fixed size	50.0/50.0	50.0/50.0	50.0/50.0	
edgeless				
Lmin/40(Wmin)	1.6/96.0	2.0/120.0	3.0/180.0	

These sizes are intended for use in full characterization of the transistor process targets and for extraction of device model parameters. Transistor sizes marked with a # are the minimum set of transistors necessary for run acceptance or test strip purposes. In addition, the edgeless device is intended for evaluation of radiation hardness of the process.

1.2.6.1 TESTING

1.2.6.1.1 Tests performed on transistors are:

TRANSISTOR THRESHOLD VOLTAGE

Threshold voltages (Vth) are obtained form a conductivity curve which is a plot of drain current vs. gate voltage (Vg) for a drain voltage (Vd) that is much less than twice the Fermi potential (2 * phi). The absolute drain voltage is set at 50 mV. Threshold voltage is found by extrapolating the linear portion of the conductivity curve to Id = 0. The intersection of the extrapolated line is defined as the threshold voltage. Measurements must be made using at least three different body voltages (Vbs, 0.0, 2.5, and 5.0 volts).

PROCESS GAIN FACTOR

The slope of the conduction curve obtained in the threshold voltage measurement process is used to calculate the process gain factor (K') The slope (S) of the conduction curve is 2 * K * Vd. Therefore,

$$K = S / 2 * Vd.$$

Since K = K' * (W / L), then the process gain factor is calculated from K' = (S/2*Vd)*(L/W).

(Note: W and L must be corrected for as-fabricated W and L,
where W = W_drawn - DW, and L = L_drawn - DL.
W_drawn and L_drawn are measured in
EFFECTIVE CHANNEL WIDTH/LENGTH section.)

BODY EFFECT

The change in voltage threshold due to source to substrate (body) reverse bias is obtained from measurements of voltage threshold at different body reverse biases. Threshold voltages are measured at three different body voltages (0.0V, 2.5V, 5.0V; negative relative to source for N channel devices and positive relative to source for the P channel devices). Threshold voltages are measured in the manner described above.

SATURATION CURRENT

Saturation current is measured by connecting the gate to the drain (body connected to source) and applying Vgs=Vds= 5.0 volts and measuring current (Idss). The test transistor upon which this measurement is taken is: Lmin / 6(Wmin).

PUNCH THROUGH VOLTAGE

This test is performed only on short channel devices. The gate is connected to the source (body connected to source) and the drain is connected to a constant current supply. Punch through voltage (Vpt) is the resulting Vds. The test transistor is Lmin / 6(Wmin)

1.2.6.1.2 Tests performed on selected transistors include:

TRANSISTOR I/V CURVES

A selected set of tranisistors will be used to collect I/V curves for SPICE Model Parameters. Drain current (Ids) measurements will be made at various drain-source voltages (Vds), gate-source voltages (Vgs) and bulk-source voltages (Vbs). The specific set of transistor geometries and sets of bias voltages will be determined by the requirements of the parameter extractor. Provisions should be made to enter the temperature of the vacuum chuck at the time of the test either by manual entry or by automatic monitoring device.

ACTIVE AREA JUNCTION LEAKAGE

Junction leakage current is measured at a junction potential 5.0 V. Source/drain junction to well leakage is measured with the well connected to the bulk. Junction leakage will be measured on the drain of the 50/50 transistor structure with the gate and source floating.

ACTIVE AREA JUNCTION BREAKDOWN

Junction breakdown is measured by applying a reverse bias current of 1.0uA (positive for N junctions and negative for P junctions) and measuring the resulting junction voltage. Source/drain junction to well breakdown is measured with the well connected to the bulk. Measurements are made on the 50/50 transitor structure using the drain junction with the source and gate floating.

WELL JUNCTION BREAKDOWN

Well junction breakdown is measured by applying a reverse bias current of 1.0uA (positive for N junctions and negative for P junctions) and measuring the resulting junction voltage. Well to bulk junction breakdown will be measured on the the 50/50 transistor structure with the gate, drain and source connected to the well, and using the wafer chuck as the connection to the bulk. Since the well junction breakdown voltage tends to be large, it is possible that the parametric tester maximum current force compliance limit will be exceeded. In order to reduce the possibility of labeling a well junction as faulty (due to open connections to it) a test for rectifying junction must be performed before testing the

well junction breakdown. Then if the parametric tester maximum compliance limit is exceeded the test report can at least indicate that the breakdown voltage exceeds this limit.

DRAIN/SOURCE LEAKAGE

Drain/source leakage (Ids0) is measured with the gate connected to the source (body connected to source) and Vds= 5.0 volts. The transistor with length = Lmin and width = 40(Wmin) will be used for the leakage measurement. Measurements are made with gate and bulk connected to ground and a picoammeter connected between source and ground.

SUBTHRESHOLD CHARACTERISTICS

Subthreshold drain current is measured at Vds = 5.0V (body connected to source) and at Vgs ten equally spaced voltages between 0.0 and Vth. These measurements are performed only on the Lmin/40Wmin transistor. Measurements are made with bulk connected to ground and a picoammeter connected between source and ground. The subthreshold slope (in Decades/Volt) and correlation coefficient is calculated using linear regression.

EFFECTIVE CHANNEL WIDTH/LENGTH

Effective channel width and length are measured by extrapolation of the channel conductance of the as fabricated and the as drawn transistors. A value of the effective channel length and width is obtained by adding the delta length and delta width values to the drawn length and width. The transistors required for the delta_L measurement are: 25/2(Lmin)/6(Wmin) and 5/2(Lmin)/6(Wmin). The transistors required for the delta_W measurement are: 8(Lmin)/10(Wmin) and 8(Lmin)/2(Wmin).

Delta Channel Length: $DL = (L1*S1 - L2*S2) / (S1 - S2)$,

for transistors with: $W1 = W2$

Delta Channel Width: $DW = (W1*S2 - W2*S1) / (S2 - S1)$,

for transistors with: $L1 = L2$

where:
- S1 = linear region slope of the larger device
- S2 = linear region slope of the smaller device
- L1 = drawn device length, larger device
- L2 = drawn device length, smaller device
- W1 = drawn device width , larger device
- W2 = drawn device width, smaller device

Note:
- L_effective = L_drawn - DL
- W_effective = W_drawn - DW

1.2.7 THICK (FIELD) OXIDE TRANSISTORS

Thick oxide transistors consist of minimum active - to - active regions with the gap between them covered by metal1, metal2 or poly. In addition, a thick oxide transistor may be constructed with P-well (for P-well runs) to P+ regions at minimum spacing, covered by metal1, metal2, or poly. In this test device the P-well is the source.

1.2.7.1 TESTING

The threshold of the thick oxide devices are measured by a single point method. The drain is connected to the overlapping gate and a constant current source at iforce = 1.0uA is connected to the drain. The resulting voltage is measured and reported as the threshold.

1.2.8 VARIABLE RATIO INVERTERS

Inverters constructed with minimum channel length P and N channel transistors are contained in a group with common Vdd, Ground and inputs, separate outputs, and with ratios of 1.0, 1.5, 2.0. Channel lengths are Lmin and N channel widths are set to 2(Wmin).

1.2.8.1 TESTING

Each inverter is tested with Vdd set at the nominal operating voltage for the technology (e. g., Vdd=5.0 V. for 2.0 um CMOS). The output voltage is measured with the input connected to Vdd and Ground. The input is connected to the output and the resulting stable voltage is identified as the inverter threshold (Vinv). Finally the gain of the inverter is measured at an input voltage of Vinv.

1.3 AC PARAMETRIC TEST STRUCTURES

At the present the only AC parameters that will be monitored are the interlayer capacitances. At some later time the transistor small signal characteristics may be monitored.

The capacitor array consists of area capacitors (small perimeter), fringe capacitors (large perimeter), edge (net - net) capacitors, and crossover capacitors. In all cases, the capacitance measurements require further data reduction to render the desired information (e.g., extraction of the area component and the fringe component of capacitance). This data reduction is done in the report generator.

Topologically, all capacitors are designed to fit into the 2 x 10 pad block height of 240 um. The lengths of the capacitor structures are varied to obtain the desired capacitance, but are currently fixed at 300um. A full four point electrical structure is maintained to maximize the accuracy that is available from a general purpose LCR meter.

Capacitors that have one electrode connected to the well (either P-well or N-well) will have a substrate to well strap to assure that the stray capacitance can be compensated by one of the two calibration capacitors.

1.3.0.1 NULL CAPACITOR (Calibration Capacitor)

Two four pad "null" capacitors are provided on the dropin to measure and store the stray capacitance associated with the test fixture for deduction from subsequent measurements. These two calibration capacitors are configured topologically to occupy two adjacent 2 x 2 slots in the capacitor array section of the PCM die. One calibration capacitor is floating so it can be used to calibrate out stray capacitances involved in measuring capacitors that do not have one electrode connected to the substrate (e.g., a metal1 to metal1 edge capacitor). The other calibration capacitor has one electrode connected to the substrate to calibrate out stray capacitances that are seen when measuring capacitors that use the substrate as one electrode (e.g., metal2 to substrate).

1.3.1 AREA CAPACITORS

The area capacitors are designed with the top electrode dimensions set at 240 um high by 300 um wide. This provides at least 1.0 pF capacitance from the field oxide capacitors.

1.3.1.1 TESTING

Measurements are made with an AC test voltage of 100mV rms and a frequency of 1.0MHz. Other test requirements, as yet undefined, could require other values of test voltage and test frequency.

Basic thin oxide capacitor measurements for the purposes of determining the thickness of the gate oxide will use a bias potential of magnitude and sign that will cause heavy inversion of the oxide semiconductor interface. Since thin oxide capacitors are essentially large area transistors with drain and source connected together the bias voltage magnitude is determined by the process target operating voltage.

All other capacitors are tested at zero bias voltage.

Geometrical parameters are:

Area: Aa = H * L um**2

Perimeter: Pa = (2 * H) + (2 * L) um

where H = top electrode height
L = top electrode length

Thin oxide capacitor measurements are used in the computation of the oxide thickness with the following equation:

Tox = (Aa * 3.3468E-11) / Cam

where Cam = measured capacitance of the area capacitor

Interlayer insulator capacitor measurements can be used to calculate the thickness of the insulator by using the above equation if the interlayer insulator is silicon dioxide. If the layer insulation is some other material (e.g., silicon nitride or combination of both) the more general form of the equation must be used:

Tins = E * E0 * (Aa / Cam)

where E = effective dielectric constant of the insulator

and E0 = permitivity of free space = 8.854e-12 Farad/m

1.3.2 FRINGE CAPACITORS

The fringe capacitors are comb structures with a comb width of 10 um and a comb spacing of 10um. The height is slightly smaller than 240 um, the maximum height permitted by the capacitor structures. Top electrode length is 300 um.

1.3.2.1 TESTING

Measurements are made with an AC test voltage of 100mV rms and a frequency of 1.0MHz. Other test requirements, as yet undefined, could require other values of test voltage and test frequency.

Capacitors with thin oxide between the layers must be measured at zero volts bias to obtain the gate overlap capacitance.

Junction capacitors are measured with a zero bias voltage.

Field oxide capacitors are measured with a voltage applied to cause strong accumulation. The magnitude of this voltage is determined by the technology (e. g., for 3.0 um CMOS the voltage is 10 volts).

Geometrical parameters are:

Area: Af = (NR * H * 10) + ((NR - 1) * 10 * 10) um**2

Perimeter: Pf = (H * 2) + (NR * 2 * 10) + ((NR - 1) * 2 * H) um

where NR = INT(L / 20)
H = top electrode height
L = top electrode length

Computation of component capacitances (e.g., junction: CJSW and CJ) using the area capacitor measurements and the fringe capacitor measurements is done with the following equations:

Fringe capacitance:

$$Cf = ((Cam/Aa) - (Cfm/Af)) / ((Pa/Aa) - (Pf/Af)) \qquad pF/um$$

Area capacitance:

$$Ca = (Cam/Aa) - Cf*(Pa/Aa) \qquad pF/um**2$$

where Cam = measured capacitance on the area capacitor
Cfm = measured capacitance on the fringe capacitor

1.3.3 EDGE (NET TO NET) CAPACITORS

Net to net capacitors are intended to directly measure the capacitance between parallel runs of wires in the same layer with minimun design rule spacing. These capacitors are interdigitated double combs (fish bone structures) with minimum wire width and spacing. This topology minimizes parasitic resistance in series with the capacitance being measured.

These capacitors are generated for only metal1, metal2 and polysilicon. There is an maximum integer number of comb structures computed to fit within a length of 300 um.

1.3.3.1 TESTING

Measurements are made with an AC test voltage of 100mV rms and a frequency of 1.0MHz. Other test requirements, as yet undefined, could require other values of test voltage and test frequency.

Capacitances are measured at zero bias voltage.

Geometrical parameters are:

Edge Length: $Le = 2*N*((H - 10) + (W * 2) + (S * 2))$

where S = min. design rule spacing
W = min. design rule width
N = INT(L / (2*W + 2*S))
H = top electrode height
L = top electrode length

Edge capacitance:

$$Ce = (Cem / Le) \qquad pF/um$$

where Cem = measured capacitance on the edge capacitor

1.3.4 CROSSOVER CAPACITORS

The crossover capacitance tests consist of crossings of Metal1, Metal2 and Metal1, Poly to measure the total capacitance per crossing. They consist of parallel runs of the lower layer crossed by orthogonal runs of the upper layer. The sizes and number of crossings are used to compute the "excess capacitance" per crossing that would be predicted from just the area capacitance contribution. The number of crossings is determined by the upper electrode length and the layer (the height is 240 um) and is generated by filling the available space with the maximum integer number of upper and lower layer runs that is allowed by

the space available.

1.3.4.1 TESTING

Measurements are made with an AC test voltage of 100mV rms and a frequency of 1.0MHz. Other test requirements, as yet undefined, could require other values of test voltage and test frequency.

Geometrical parameters are:

Number of crossings:

$Nc = Nx * Ny$

where
$Nx = INT(L / (W2 + S2))$
$Ny = INT((H + W1) / (W1 + S1))$
$S1$ = min. design rule spacing of top electrode
$W1$ = min. design rule width of top electrode
$S2$ = min. design rule spacing of bottom electrode
$W2$ = min. design rule width of bottom electrode
H = top electrode height
L = top electrode length

Crossover capacitance:

$Cc = (Ccm / Nc)$ pF/um

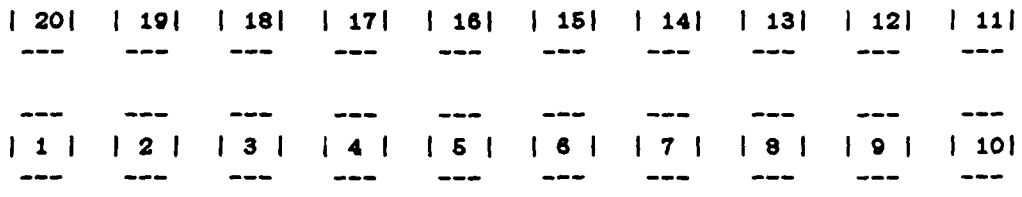
where Ccm = measured capacitance on the crossover capacitor

1.4 FUNCTIONAL TEST STRUCTURES

The functional test structures are intended to be used to evaluate the performance of the extracted model parameters and to act as an alarm for a low yield fabrication run if there are serious flaws in fabrication.

They will provide performance information on the standard cell circuits present on the run.

The parametric test area is configured so that the pin-out is standardized to minimize the complexity of the interface to test equipment. This pin-out is defined assuming the following pin numbering convention:



Assigned pin functions are defined as follows:

Pin #	Function
1	Clock
2	Input/Output
3	Input/Output
4	Input/Output
5	Input/Output
6	Input/Output

7	Input/Output
8	Input/Output
9	Input/Output
10	Ground
11	Input/Output and Ring Oscillator ENABLE
12	Input/Output
13	Input/Output
14	Input/Output
15	Input/Output
16	Input/Output
17	Input/Output
18	Input/Output
19	Ring Oscillator Output
20	Vdd

The Input/Output pins and the Clock are interfaced with the Test Pods that are connected with the functional tester. The drive lines of these Pods are tristatable and are parallelled with the Acquisition Pods to permit flexable utilization of the 16 functional I/O pins. Pin 11 is also connected to a small relay that can connect the Ring Oscillator ENABLE signal to this pin. The purpose of the relay is to reduce the stray capacitance associated with the ENABLE signal wire.

1.4.1 RING OSCILLATOR

The ring oscillator is a 31 stage string of inverters with a ratio of two. The inverter transistors have a N channel width of twice minimum and a channel length of minimum. The inverter ring is buffered with three stages of geometrically growing inverters such that it is capable of driving the interconnect capacitance to the frequency counter buffer. This buffer is a unity gain amplifier with 100 MHz bandwidth and a capability of driving a coaxial cable with a 50-Ohm termination.

1.4.1.1 TESTING

The parametric tester supplies power (Vdd and ground) to the device under test through the probe card interface board. A relay is activated to connect a parametric tester pin to the ring oscillator enable pin and a disable voltage (equal to Vdd) is applied to supress any multimode oscillation that may be present. The disable voltage is removed to start oscillation and a frequency measurement is taken.

The IEEE bus is used to command up to five measurements of frequency from the frequency counter. The parametric tester will compute the average of two consecutive frequency measurements in which the second reading is within 10% of the first. Up to five readings are taken until the above condition is achieved. If acceptable readings are not found then the structure is considered inoperative.

The parametric tester will report the average of two frequency measurements.

1.4.2 DYNAMIC SHIFT REGISTER

The dynamic shift register is a master - slave two phase clocked shift register that is eight bits wide and six words long. The two phase clock (with complements) is generated in the test structure. The functional tester need only provide data and a single phase clock that is true when data is stable.

1.4.2.1 TESTING

The shift register is supplied Vdd and Ground from the parametric tester and is clocked at 1.0 MHz by the functional tester to determine if it is functioning. The supply current is logged for future reference during data reduction.

If the Dynamic Shift Register is fully functional a value of 1.0 is logged and if it is not functional a value 0.0 is logged. No attempt is made to log the failure pattern.

1.4.3 PATTERN GENERATOR

The pattern generator is a 511 bit maximum length pseudorandom number generator constructed from CMOS3 Library standard cells (or equivalents). The cells used are:

XOR (2310)
D-FF with S/RESET (1480)
INVERTER PAIR (1100)
NON-INVERTING OUTPUT BUFFER (1510)

It is a modular shift register generator with 9 stages with feedback from the 9th stage modulo-2 added with the output of 6th, 4th, 3rd, 2nd and 1st stages and fed to the inputs of 7th, 5th, 4th, 3rd and 2nd stages, respectively. A logic diagram illustrating the setup is as follows: (see figure)

(Figure not available on-line)

1.4.3.1 TESTING

The pattern generator is clocked at 1 MHz and its output tested for the expected sequence of bits.

If the Pattern Generator is fully functional a value of 1 is logged and if it is not functional a value of 0 is logged. No attempt is made to log the failure pattern.

Appendix I - Test structure nomenclature IDs

Test structures on MOSIS generated process monitors have nomenclature identification. These IDs help locate a particular structure within the process monitor. The following lists the test structures titles and their corresponding ID.

Test Block Title	ID
Alignment bridge METAL1 to P_PLUS_ACTIVE in Y	A1
Alignment bridge CUT to N_PLUS_ACTIVE in X	A2
Alignment bridge CUT to N_PLUS_ACTIVE in Y	A3
Alignment bridge METAL1 to POLY_N_PLUS in X	A4
Alignment bridge METAL1 to POLY_N_PLUS in Y	A5
Alignment bridge CUT to POLY_P_PLUS in X	A6
Alignment bridge CUT to POLY_P_PLUS in Y	A7
Alignment bridge METAL2 to METAL1 in X	A8
Alignment bridge METAL2 to METAL1 in Y	A9
Alignment bridge VIA to METAL1 in X	A10
Alignment bridge VIA to METAL1 in Y	A11
Alignment bridge METAL1 to P_PLUS_ACTIVE in X	A12
Alignment bridge METAL1 to ELECTRODE in X	A20
Alignment bridge METAL1 to ELECTRODE in Y	A21
Alignment bridge CUT to ELECTRODE in X	A22
Alignment bridge CUT to ELECTRODE in Y	A23
Crossover Capacitor METAL2 to METAL1	C1
Crossover Capacitor METAL1 to POLY	C2
Edge Capacitor POLY to POLY	C3
Edge Capacitor METAL2 to METAL2	C4
Edge Capacitor METAL1 to METAL1	C5
Fringe Capacitor POLY to N_PLUS_ACTIVE	C6
Fringe Capacitor POLY to P_PLUS_ACTIVE	C7
Fringe Capacitor N_PLUS_ACTIVE to P_WELL	C8
Fringe Capacitor P_PLUS_ACTIVE to N_WELL	C9
Area Capacitor METAL2 to POLY	C10
Area Capacitor METAL1 to POLY	C11
Area Capacitor METAL2 to METAL1	C12
Area Capacitor METAL2 to N_PLUS_ACTIVE	C13
Area Capacitor METAL1 to N_PLUS_ACTIVE	C14
Area Capacitor METAL2 to N_WELL	C15
Area Capacitor METAL1 to N_WELL	C16
Area Capacitor POLY to N_WELL	C17
Area Capacitor N_PLUS_ACTIVE to P_WELL	C18
Area Capacitor P_PLUS_ACTIVE to N_WELL	C19
Area Capacitor POLY to N_PLUS_ACTIVE	C20
Area Capacitor POLY to P_PLUS_ACTIVE	C21
Calibration Capacitor with connected substrate	C22
Calibration Capacitor floating	C23
Area Capacitor ELECTRODE to POLY	C30
Area Capacitor METAL1 to ELECTRODE	C31
Area Capacitor METAL2 to ELECTRODE	C32

Dynamic Shift Register	F1
Pattern Generator	F2
Ring Oscillator	F3
XOR tree	F4
Ring Oscillator trio	F6
Ring Oscillator pair	F7
Test inverter(s)	I1
Poly (P+) bridge	K1
Poly (N+) bridge	K2
P+ Active bridge	K3
N+ Active bridge	K4
Metal bridge	K5
Second_metal bridge	K6
P-Well bridge	K7
N-Well bridge	K8
P+ Active to Metal contact	K9
Second Metal to First Metal contact	K10
Poly bridge	K11
Poly (P+) to Metal contact	K12
Poly (N+) to Metal contact	K13
N+ Active to Metal contact	K14
P-Well under Poly bridge	K15
N-Well under Poly bridge	K16
Electrode bridge	K20
Electrode to Metal contact	K21
Latchup Beta Transistors	L1
Step coverage METAL1 METAL2	S1
Step control METAL1 METAL2	S2
Step coverage METAL2	S3
Step control METAL2	S4
Step coverage METAL1	S5
Step control METAL1	S6
N_ENHANCEMENT common transistor(s)	T1
P_ENHANCEMENT common transistor(s)	T2
N_ACT field oxide transistors	T3
P_ACT field oxide transistors	T4
N_ENHANCEMENT isolated transistor(s)	T5
P_ENHANCEMENT isolated transistor(s)	T6
N_ENHANCEMENT closed transistor	T7
P_ENHANCEMENT closed transistor	T8

PRINTED CIRCUIT BOARDS
COST GUIDELINES

- **T/A: Going from 1 week to 4 week T/A decreases unit cost by 50%.**

- **QUANTITY: Going from a 3–board to a 25–board order decreases unit cost by 50%.**

- **LAYERS: Increasing number of layers by 2 increases unit cost by 25%.**

- **HOLE COUNT: Less than 2,000 holes/board = base price.**
  2,000 to 3,000 holes $\Longrightarrow$ Price = Base + 5%.

- **SMT: 10% higher.**

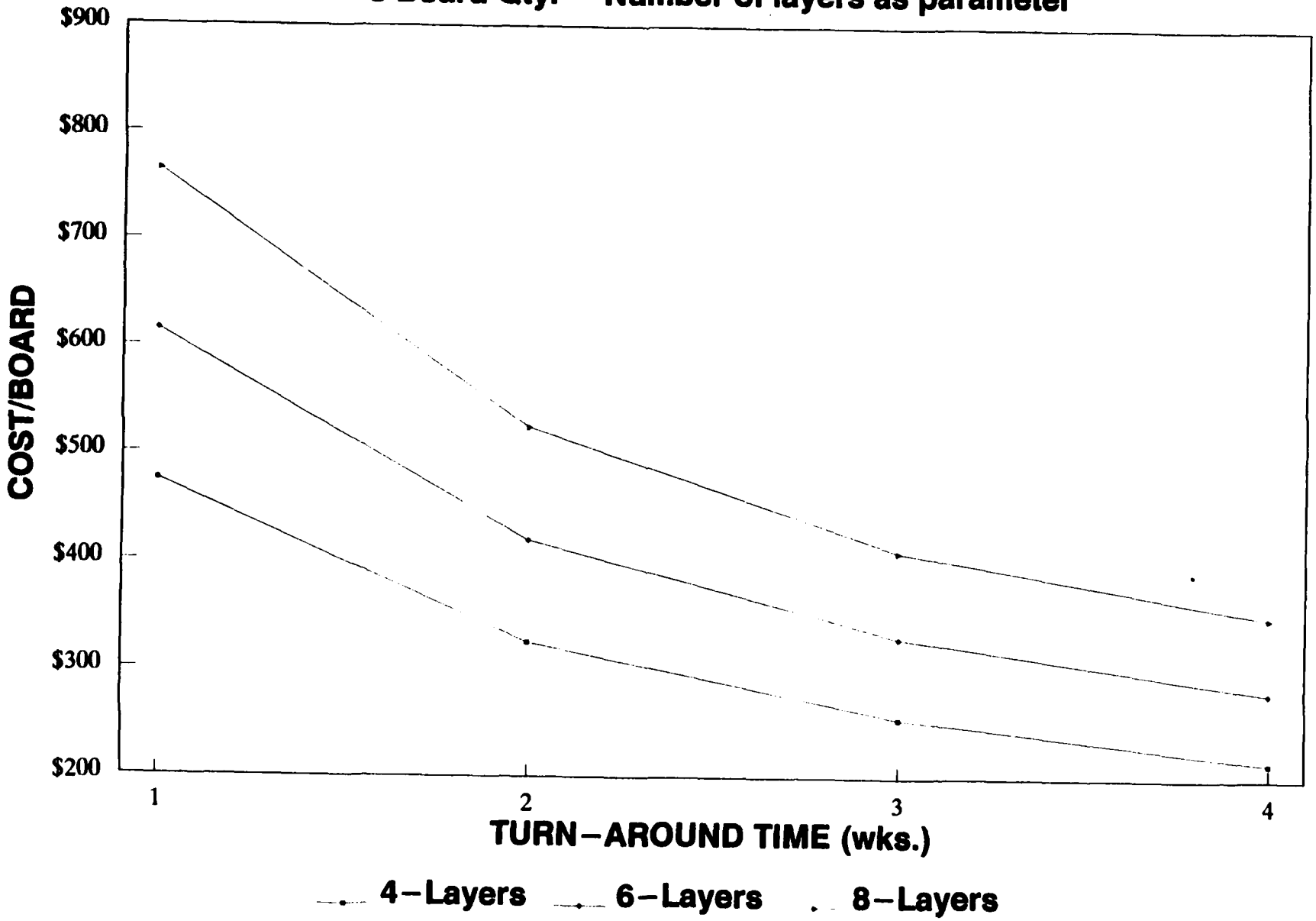
- **CONTROLLED IMPEDANCE: 20% higher.**

- **SOME TYPICAL COSTS:**
  (3 week T/A, < 2,000 holes/board)

	Unit Cost	Qty	Total Cost
• VME Bus 9" x 6", 6 layers			
Tooling	$450	1	$ 450
Fab Cost	$255	5	$1,275
Plots	$230	1	$ 230
			$1,955
• "Tiny" Board 3" x 6", 4 layers			
Tooling	$300	1	$ 300
Fab Cost	$105	5	$ 525
Plots	$155	1	$ 155
			$ 980

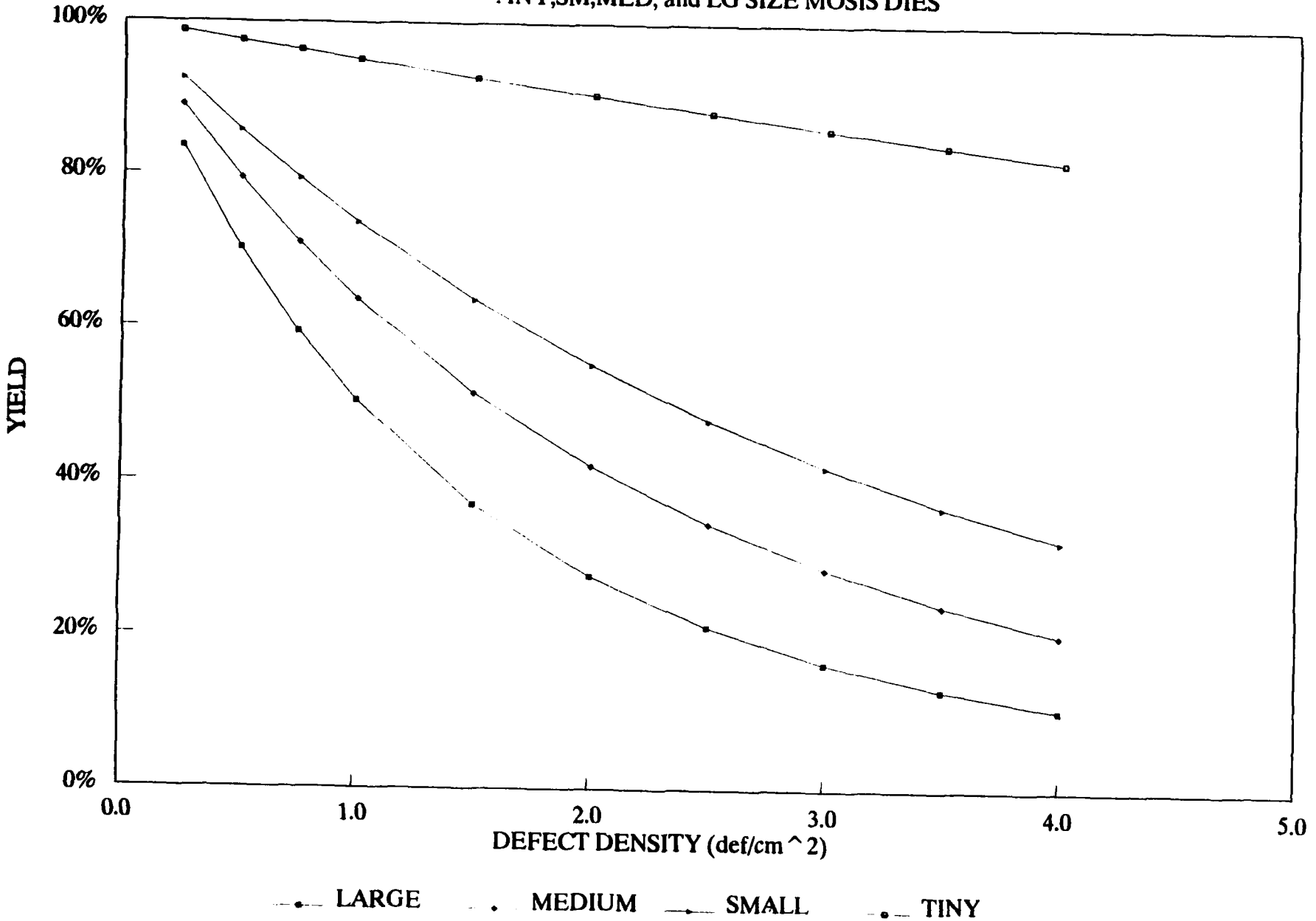
COST vs. T/A TIME (wks.)

3 Board Qty. – Number of layers as parameter



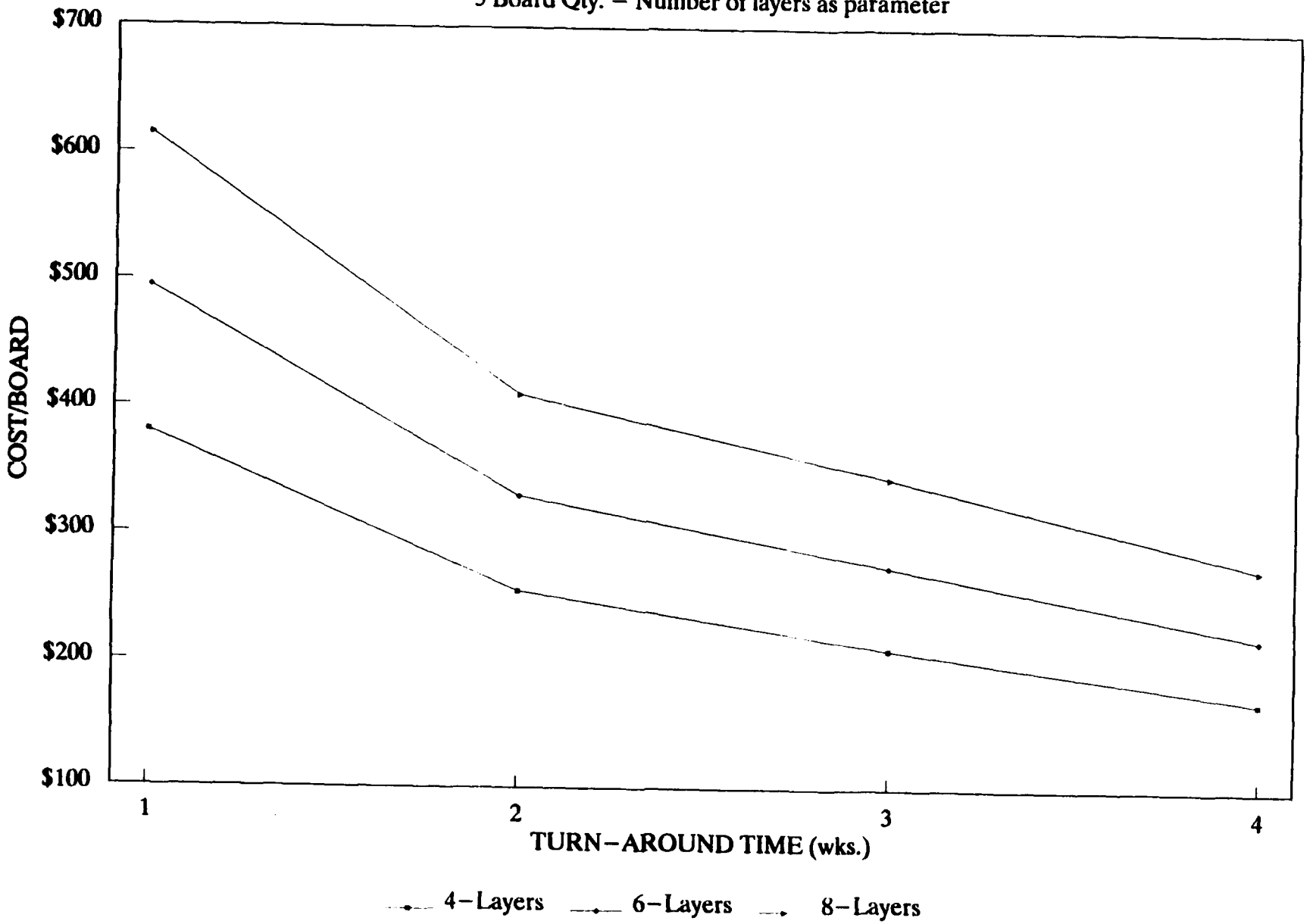
DEFECT DENSITY VS YIELD

TINY,SM,MED, and LG SIZE MOSIS DIES



COST vs. T/A TIME (wks.)

5 Board Qty. – Number of layers as parameter



PCB UNIT COST VS T/A TIME(WKS)

2WK T/A, 5BOARDS = UNITY